IBM PC felépítése

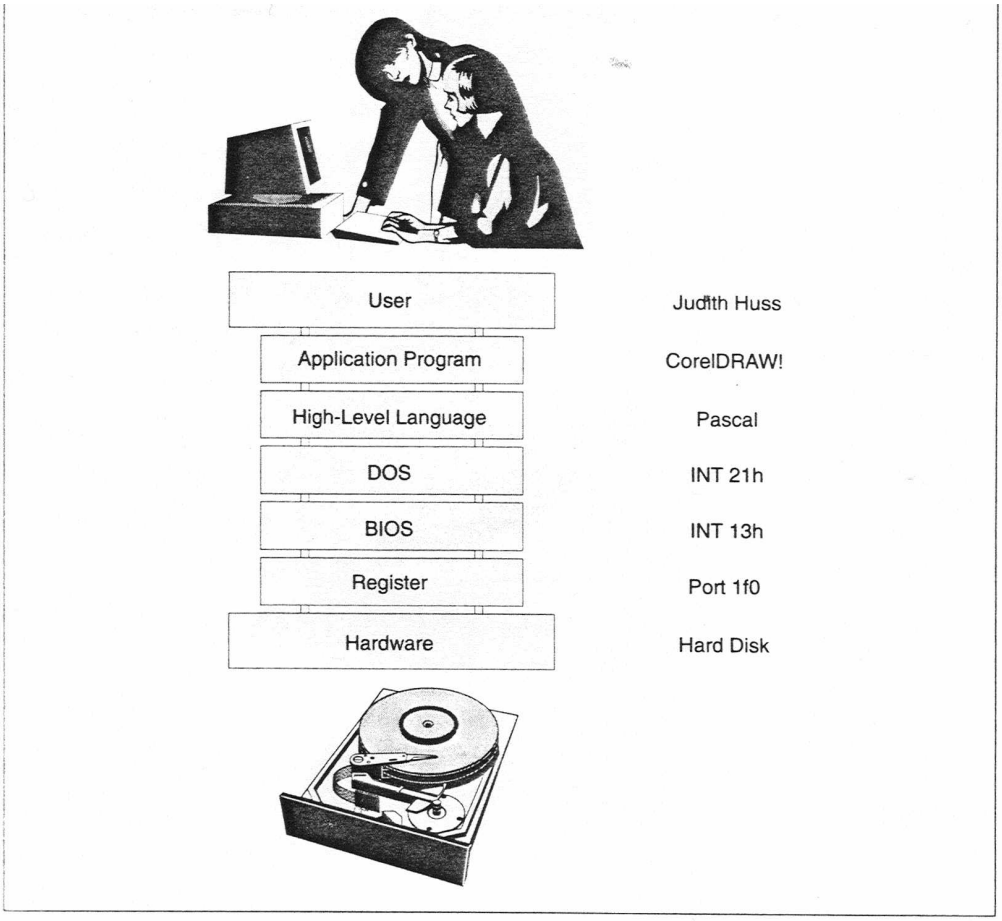


Figure 1.26: Different access levels. On the left are shown the different access levels between user and hardware. On the right is an example for each level. The top level is the application, which is the interface to the user. The bottom level is the registers that directly control the hardware.

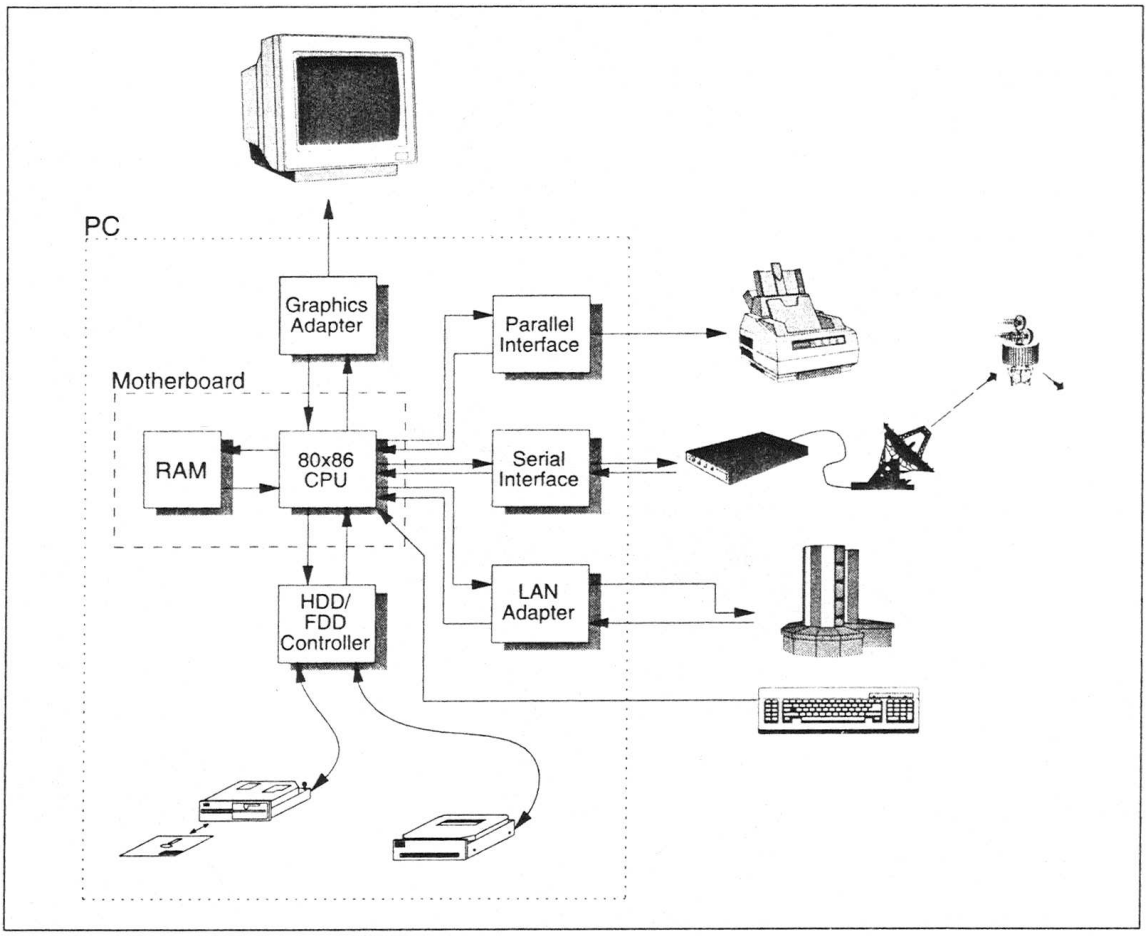


Figure 1.5: Block diagram of a PC with peripherals. The arrows indicate the direction of the data flow. The 80x86 CPU and the RAM are located on the motherboard. All parts surrounded by the broken line are normally inside the PC case.

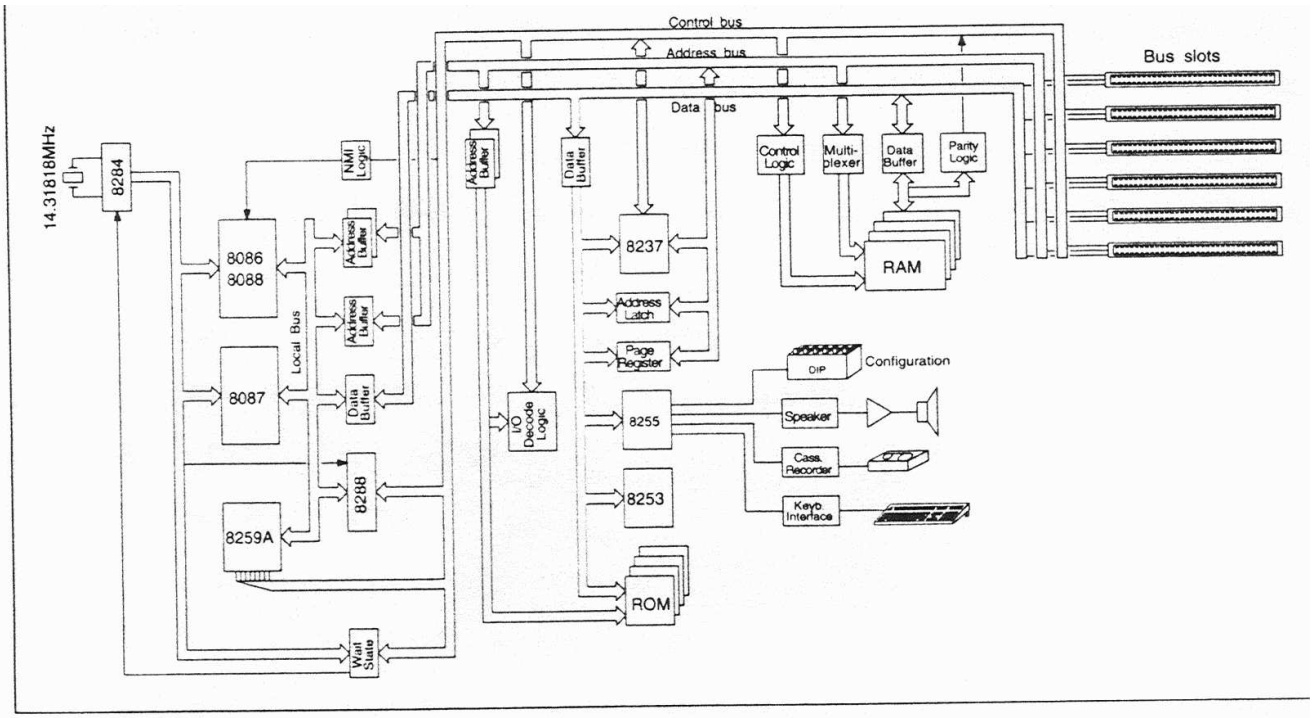


Figure 18.1: The PC/XT architecture.

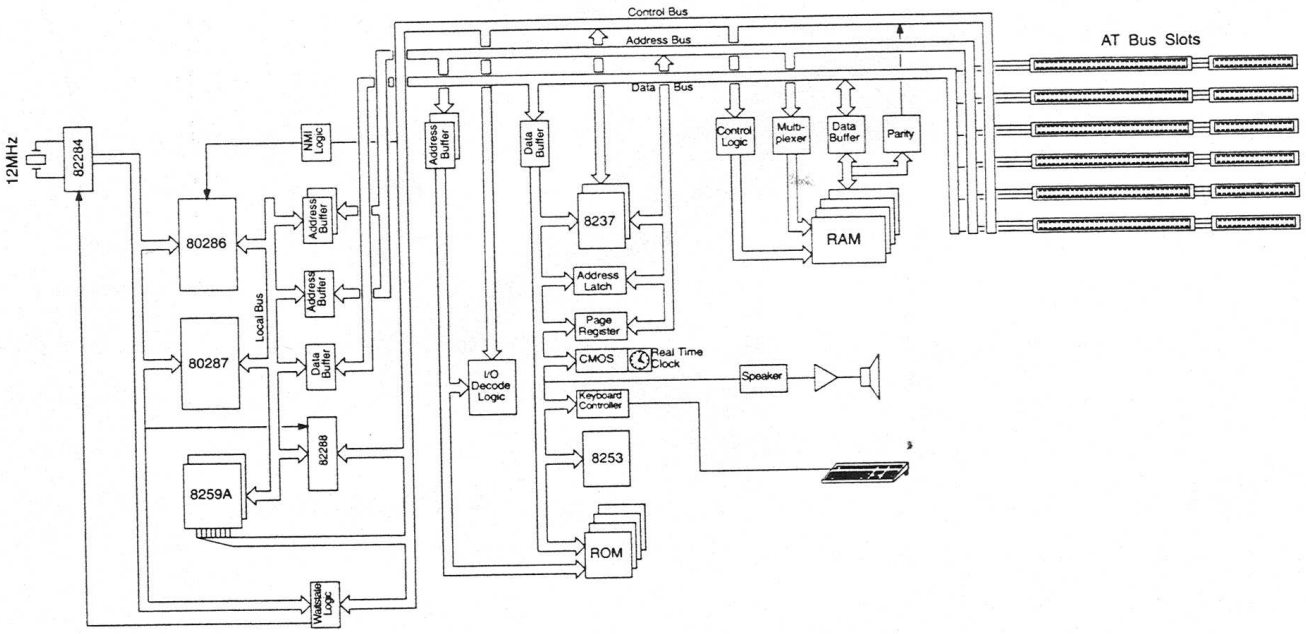


Figure 19.1: AT architecture.

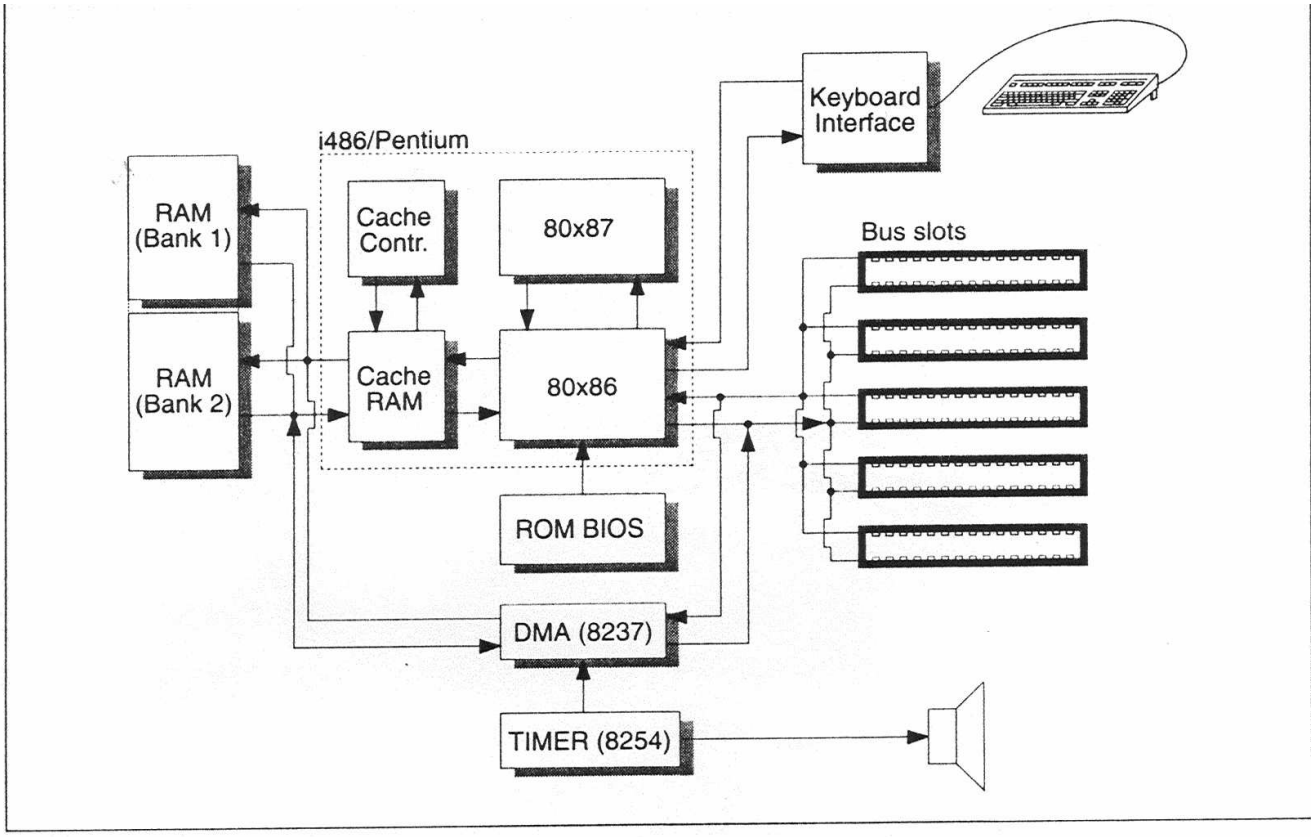
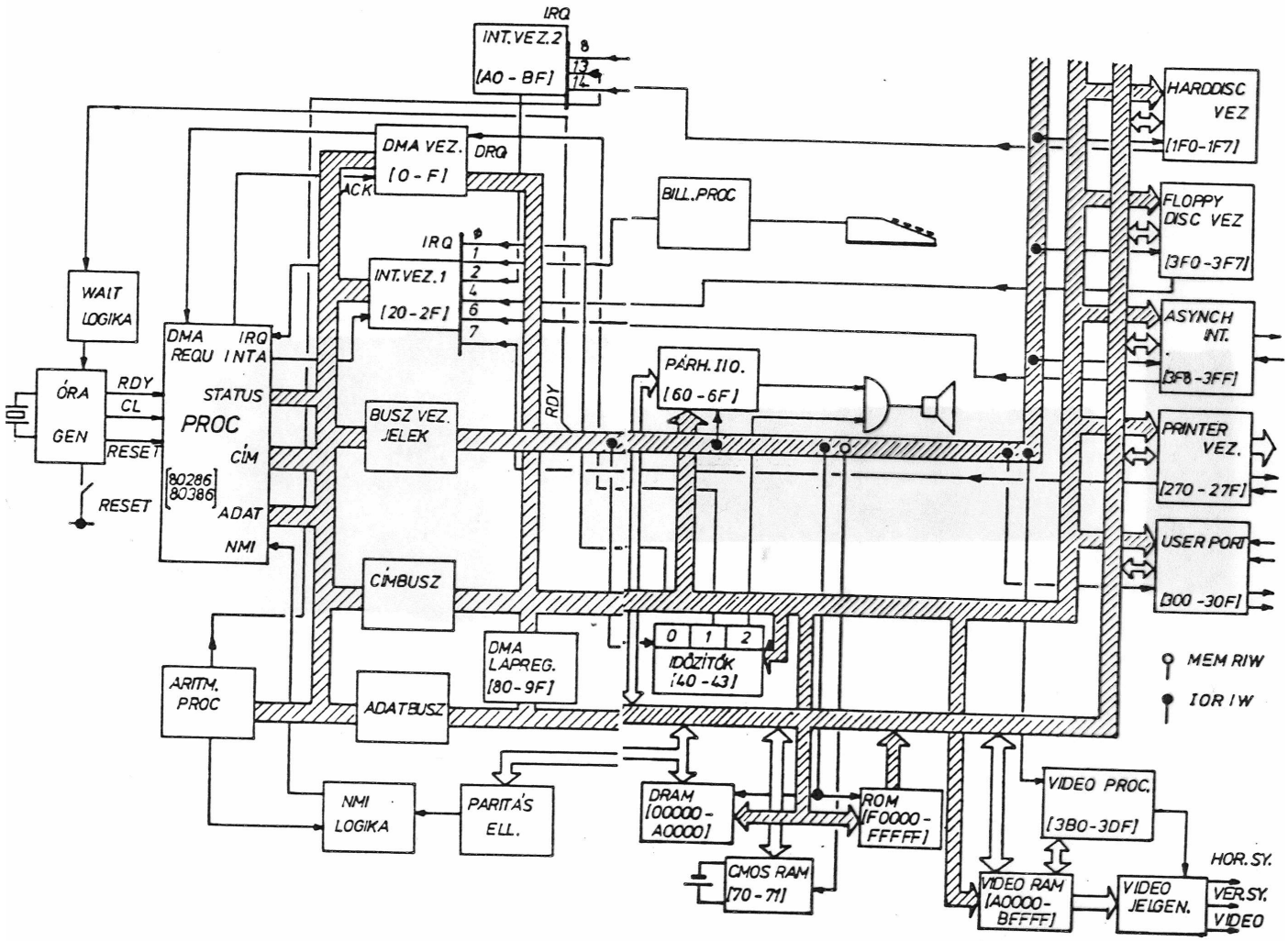
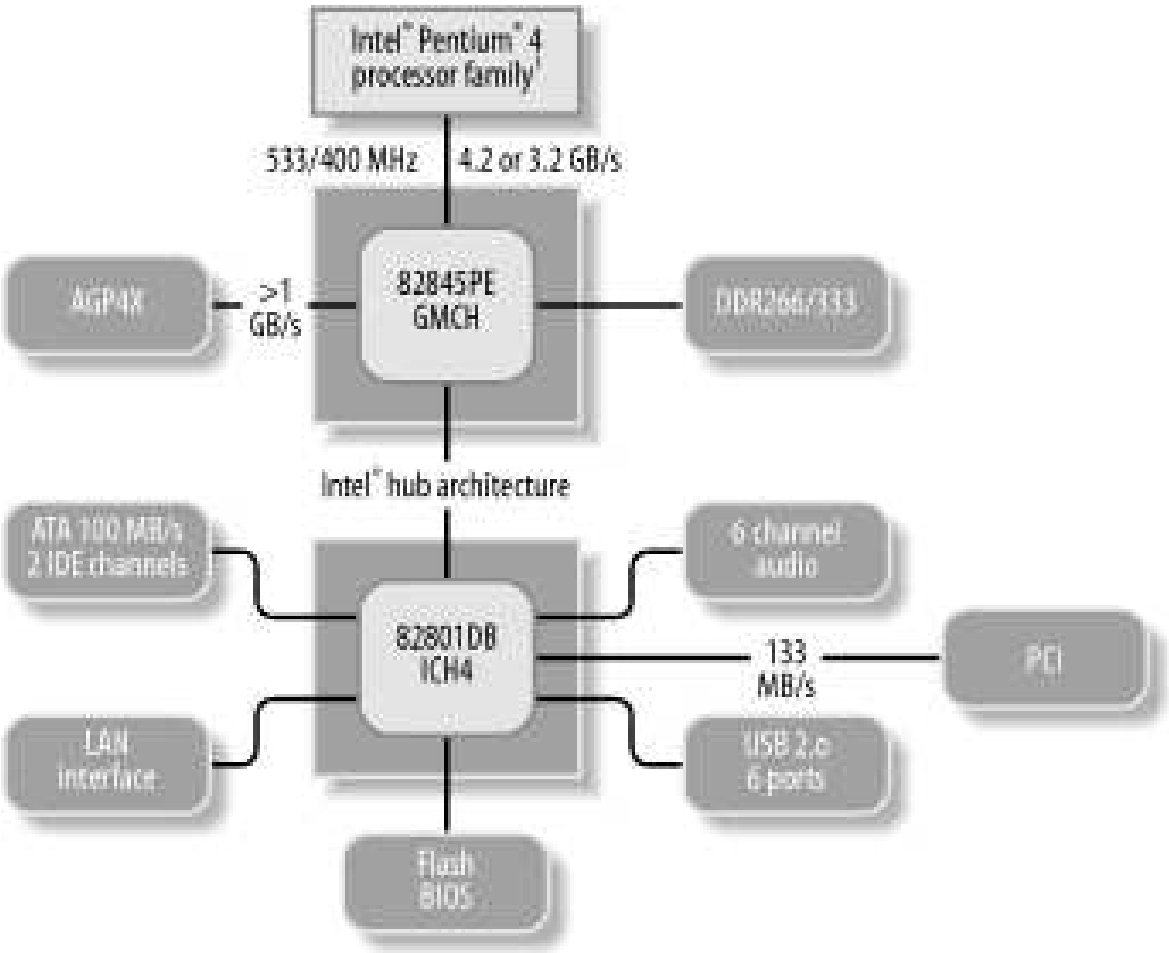
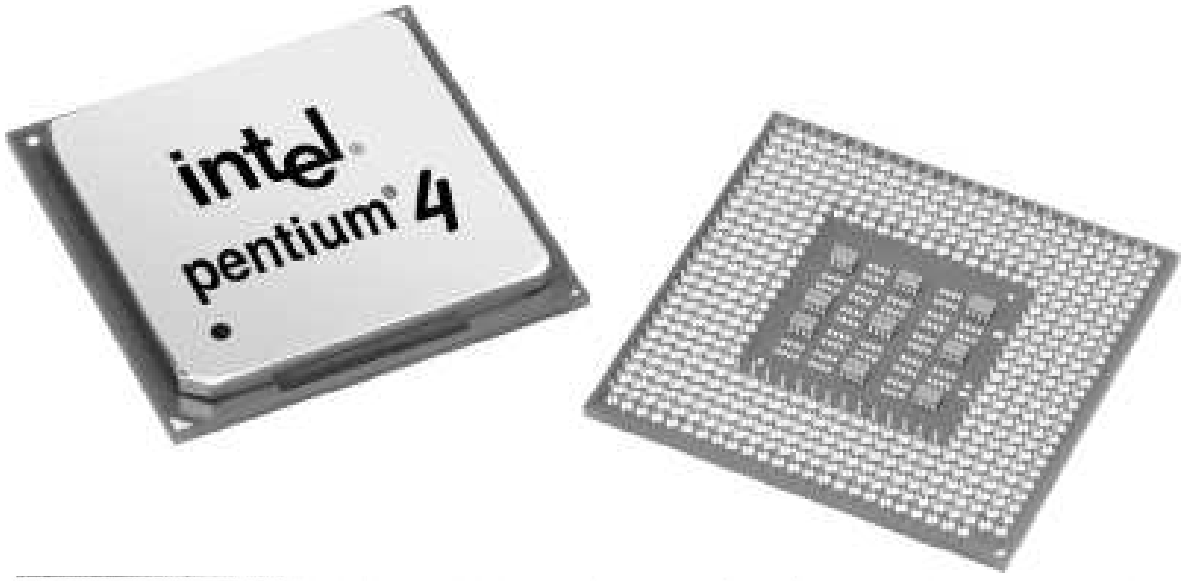


Figure 1.7: Diagram of a motherboard. The diagram shows the typical structure of a motherboard. The central part is the CPU 80x86. The CPU can be associated with an 80x87 coprocessor for mathematical applications and a cache controller and cache RAM to enhance performance. The i486 or Pentium integrates all these parts on a single chip. Additionally, on the motherboard there are the memory (RAM), the ROM BIOS, the 8237 and 8254 support chips, a keyboard interface, and the bus slots.


IRQ
INT.VEZ.2
[A0 - BF]
8
13
14
DMA VEZ.
[0 - F]
DRQ
ACK
BILL.PROC
HARDDISC VEZ
[1F0-1F7]
FLOPPY DISC VEZ
[3F0-3F7]
IRQ
INT.VEZ.1
[20-2F]
0
1
2
4
6
7
WAIT LOGIKA
ASYNCH INT.
[3F8-3FF]
DMA REQU
IRQ INTA
STATUS
PROC
CÍM
[80286 80386]
ADAT
NMI
ÓRA GEN
RDY
CL
RESET
RESET
PÁRH. IIO.
[60-6F]
BUSZ VEZ. JELEK
RDY
PRINTER VEZ.
[270-27F]
USER PORT
[300-30F]
CÍMBUSZ
0 1 2
IDŐZÍTŐK
[40-43]
DMA LAPREG.
[80-9F]
MEM R/W
IOR / W
ARITM. PROC
ADATBUSZ
VIDEO PROC.
[3B0-3DF]
NMI LOGIKA
PARITÁS ELL.
DRAM
[00000-A0000]
ROM
[F0000-FFFFF]
HOR.SY.
CMOS RAM
[70-71]
VIDEO RAM
[A0000-BFFFF]
VIDEO JELGEN.
VER.SY.
VIDEO


Intel® Pentium® 4 processor family
533/400 MHz
4.2 or 3.2 GB/s
AGP4X
>1 GB/s
82845PE GMCH
DDR266/333
Intel® hub architecture
ATA 100 MB/s 2 IDE channels
6 channel audio
82801DB ICH4
133 MB/s
PCI
LAN interface
USB 2.0 6 ports
Flash BIOS

CPU



Processor	Register width	Address bus	Data bus	Address space	Clock frequency	Used in
8088	16 bits	20 bits	8 bits	1 Mbyte	6..10 MHz	PC
8086	16 bits	20 bits	16 bits	1 Mbyte	6..10 MHz	XT,PS/2
80188	16 bits	20 bits	8 bits	1 Mbyte	6..16 MHz	–1)
80186	16 bits	20 bits	16 bits	1 Mbyte	6..16 MHz	–1)
80286	16 bits	24 bits	16 bits	16 Mbyte	12..20 MHz	AT,XT286, PS/2
i386SX	32 bits	24 bits	16 bits	16 Mbyte	16..25 MHz	AT, PS/2
i386DX	32 bits	32 bits	32 bits	4 Gbyte	16..40 MHz	AT, PS/2, EISA
i486	32 bits	32 bits	32 bits	4 Gbyte	25..50 MHz	AT, PS/2, EISA, PCI, VLB
i486DX2	32 bits	32 bits	32 bits	4 Gbyte	50..66 MHz	AT, PS/2, EISA, PCI, VLB
i486SX/i487SX	32 bits	32 bits	32 bits	4 Gbyte	25 MHz	AT, PS/2, EISA
Pentium	32 bits	32 bits	64 bits	4 Gbyte	60..99 MHz	AT, PS/2, EISA, PCI, VLB

[1] Hardly used in PCs.
PCI: PCI local bus systems
VLB: VESA local bus systems

	Covington	Mendocino	Coppermine128	Coppermine128	Tualatin
Package	SECC	SECC-2PPGA	FC-PGA	FC-PGA	FC-PGA2
Manufacturing dates	1998	1998 - 2000	2000 - 2002	2001 - 2002	2001 -
Clock speeds (MHz)	266, 300	300A, 333, 366, 400, 433, 466, 500, 533	500A, 533A, 566, 600, 633, 667, 700, 733, 766	800, 850, 900, 950, 1000, 1100	900, 1000, 1100, 1200, 1300, 1400
L2 cache size	none	128 KB	128 KB	128 KB	256 KB
L2 cache bus width	n/a	64 bits	256 bits	256 bits	256 bits
System bus speed	66 MHz	66 MHz	66 MHz	100 MHz	100 MHz
SSE instructions	--	--	✓	✓	✓
Dual CPU capable	✓	✓	--	--	--
Fabrication process	0.35µ	0.25µ	0.18µ	0.18µ	0.13µ

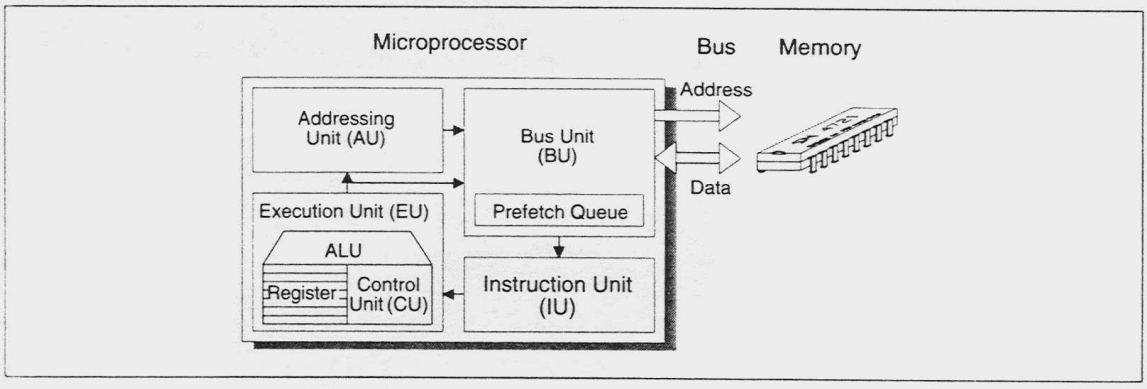
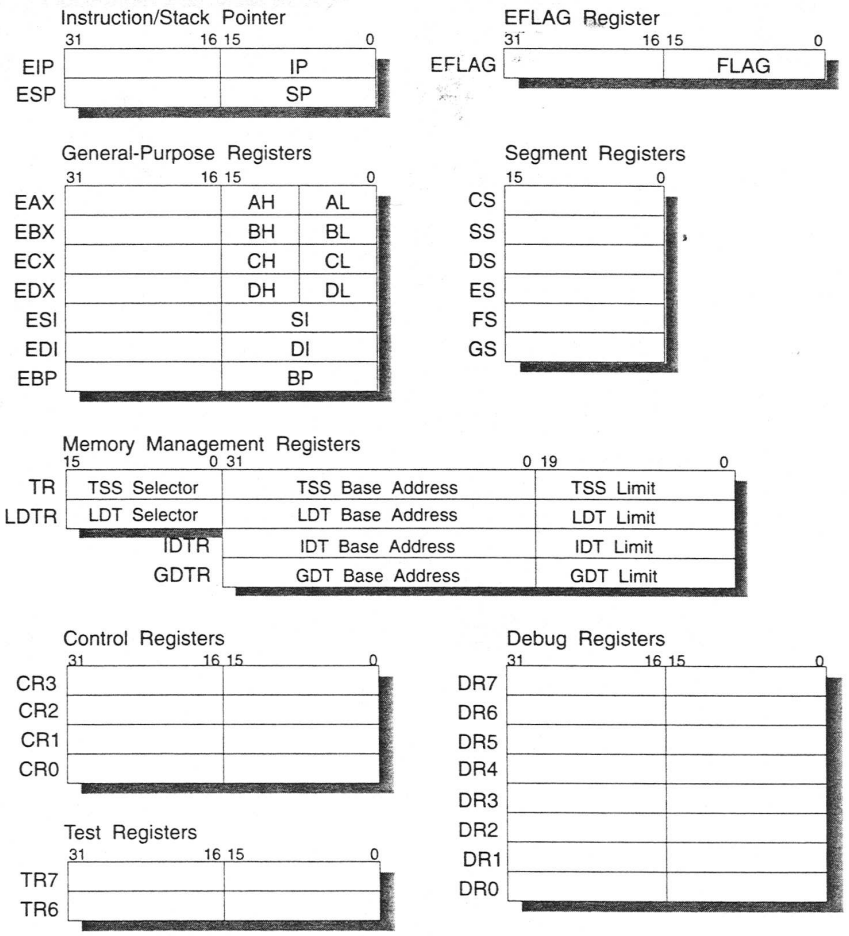


Figure 2.3: Structure of a microprocessor. A microprocessor comprises a bus interface with a prefetch queue for reading and writing data and instructions, an instruction unit for controlling the execution unit with its registers, and an addressing unit for generating memory and I/O addresses.


Instruction/Stack Pointer
31
16 15
0
EIP
IP
ESP
SP
EFLAG Register
EFLAG
FLAG
General-Purpose Registers
EAX
AH
AL
EBX
BH
BL
ECX
CH
CL
EDX
DH
DL
ESI
SI
EDI
DI
EBP
BP
Segment Registers
CS
SS
DS
ES
FS
GS
Memory Management Registers
TR
TSS Selector
TSS Base Address
TSS Limit
LDTR
LDT Selector
LDT Base Address
LDT Limit
IDTR
IDT Base Address
IDT Limit
GDTR
GDT Base Address
GDT Limit
Control Registers
CR3
CR2
CR1
CR0
Debug Registers
DR7
DR6
DR5
DR4
DR3
DR2
DR1
DR0
Test Registers
TR7
TR6

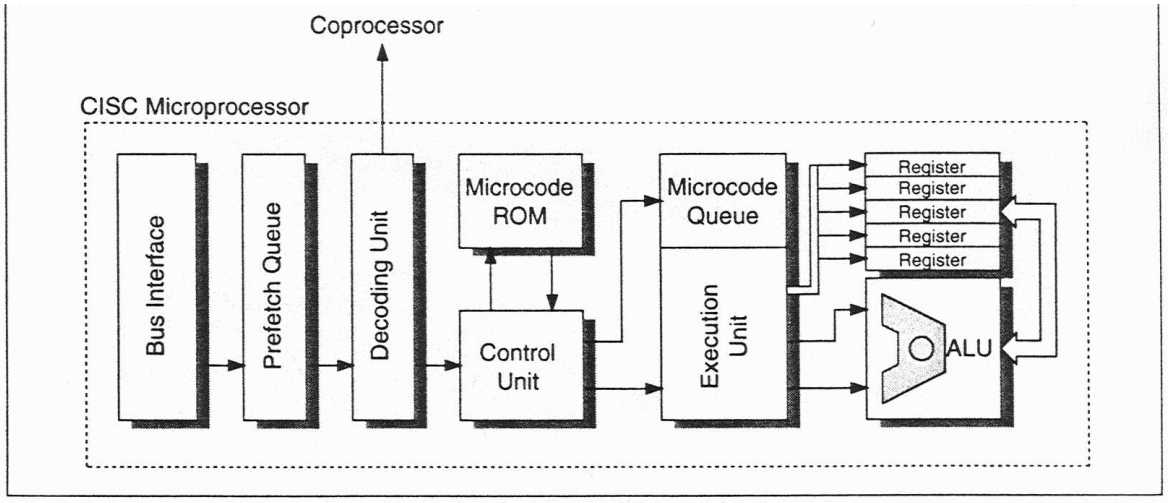


Figure 6.4: The concept of microprogramming. With microprogramming the processor fetches the instructions via the bus interface into a prefetch queue, which in turn transfers them to a decoding unit. The decoding unit decomposes a machine instruction into a number of elementary microinstructions and applies them to a microcode queue. The microinstructions are transferred from the microcode queue to the control and execution unit so that the ALU and registers are driven accordingly.

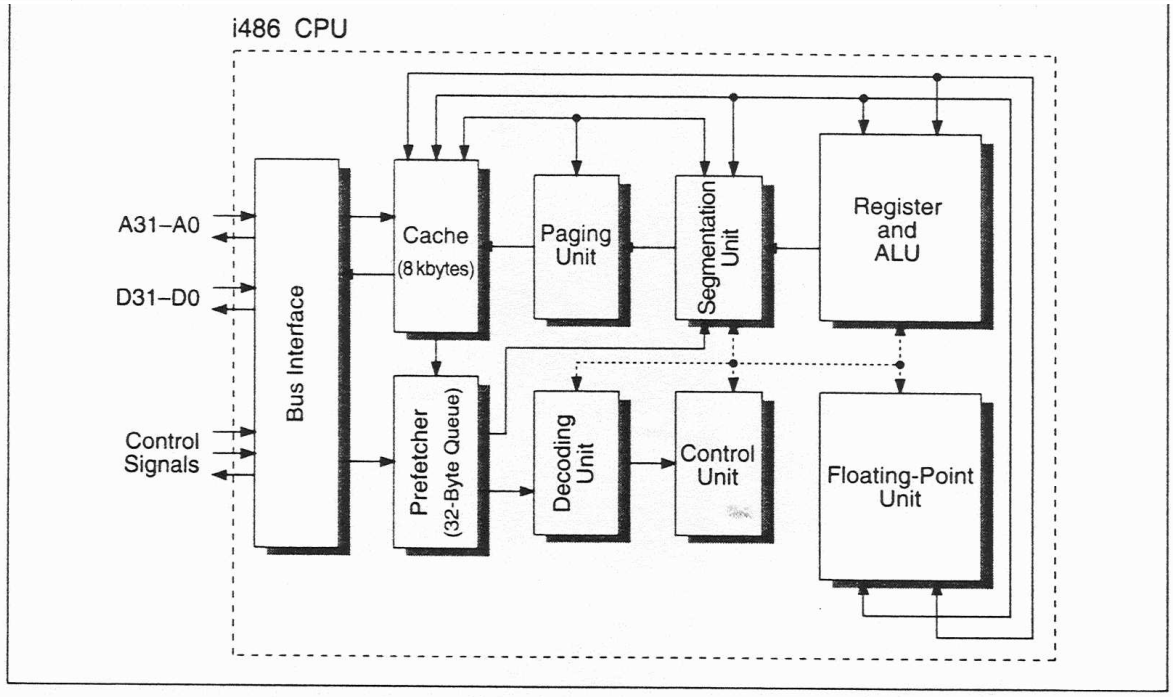


Figure 10.3: i486 internal structure. On a single chip, the i486 integrates not only an improved CPU, but also a more powerful version of the i387, a cache controller, and an 8 kbyte cache. The prefetch queue grew to 32 bytes.

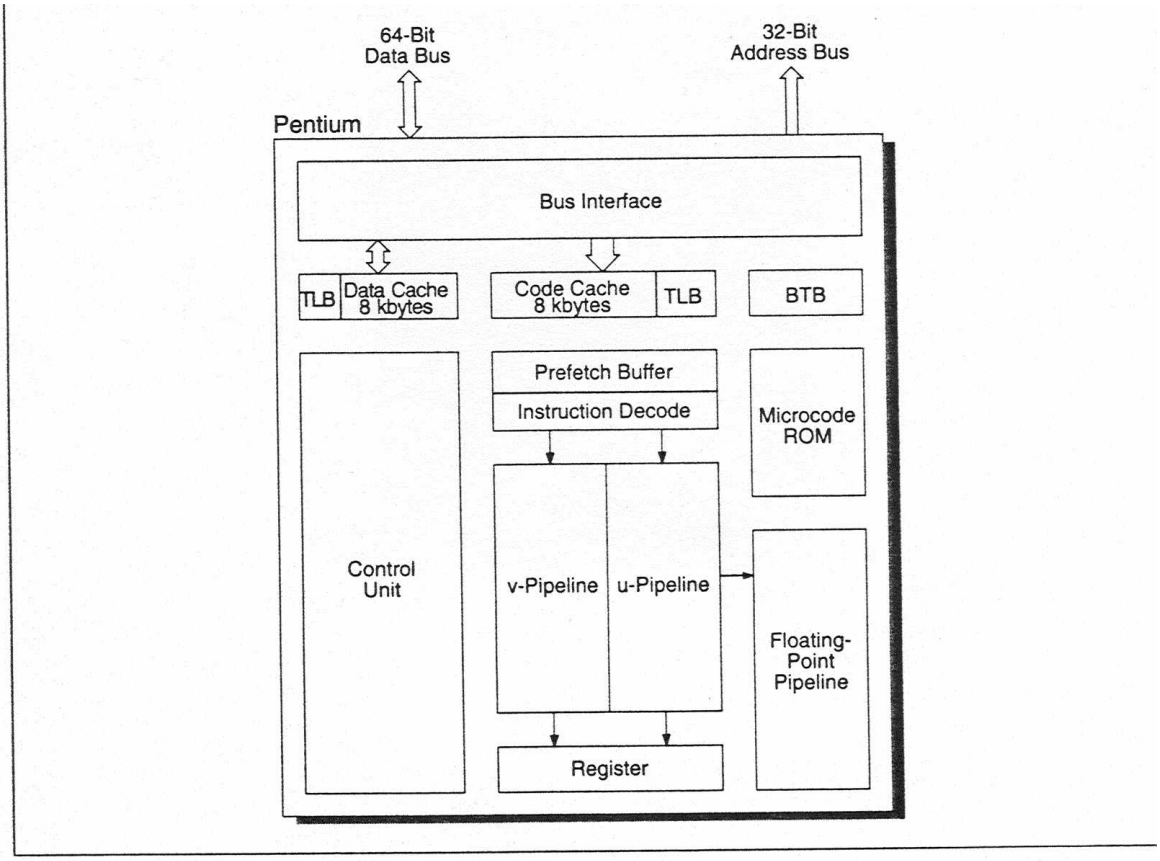


Figure 12.3: Pentium block diagram.

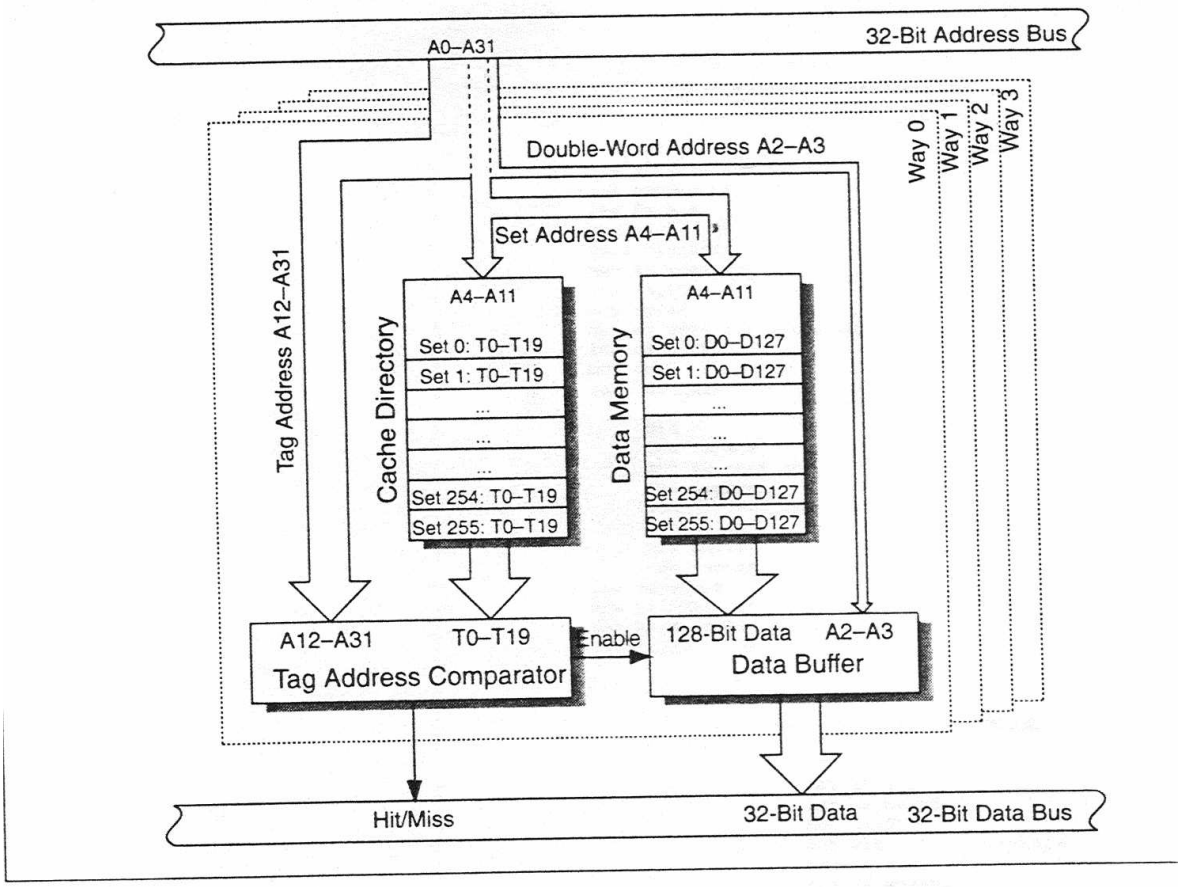


Figure 9.3: Determining cache hits.

```
mov     al,00110100B
out     timer_mode,al
sub     ax,ax
out     timer0,al
out     timer0,al


mov si,-1                   ;game-port megszolitas
mov dx,201h
out dx,al
    again:
            in al,dx        ;konverzio vege?
            inc si
            cmp si, 1500
            jg tovabb
            test al,1
            jnz again
            tovabb:
```

```
mov     al,00h
cli
out     timer_mode,al
in      al,timer0
mov     dl,al
in      al,timer0
mov     dh,al
mov     ax,max_count
sub     ax,dx
mul     timer_convert
div     ten_thousand
mov     timer_micro,ax
cmp ax,5000
jl fincsi
mov ax,5000
fincsi:
mov [datmem+bp],ax
sti
add bp,2
```

Busz vezérlés

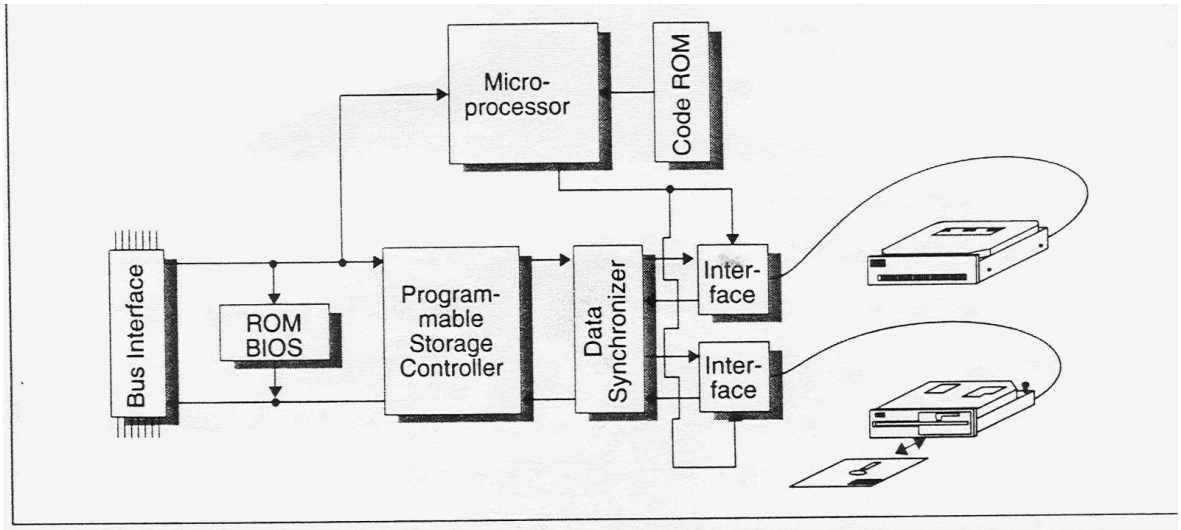
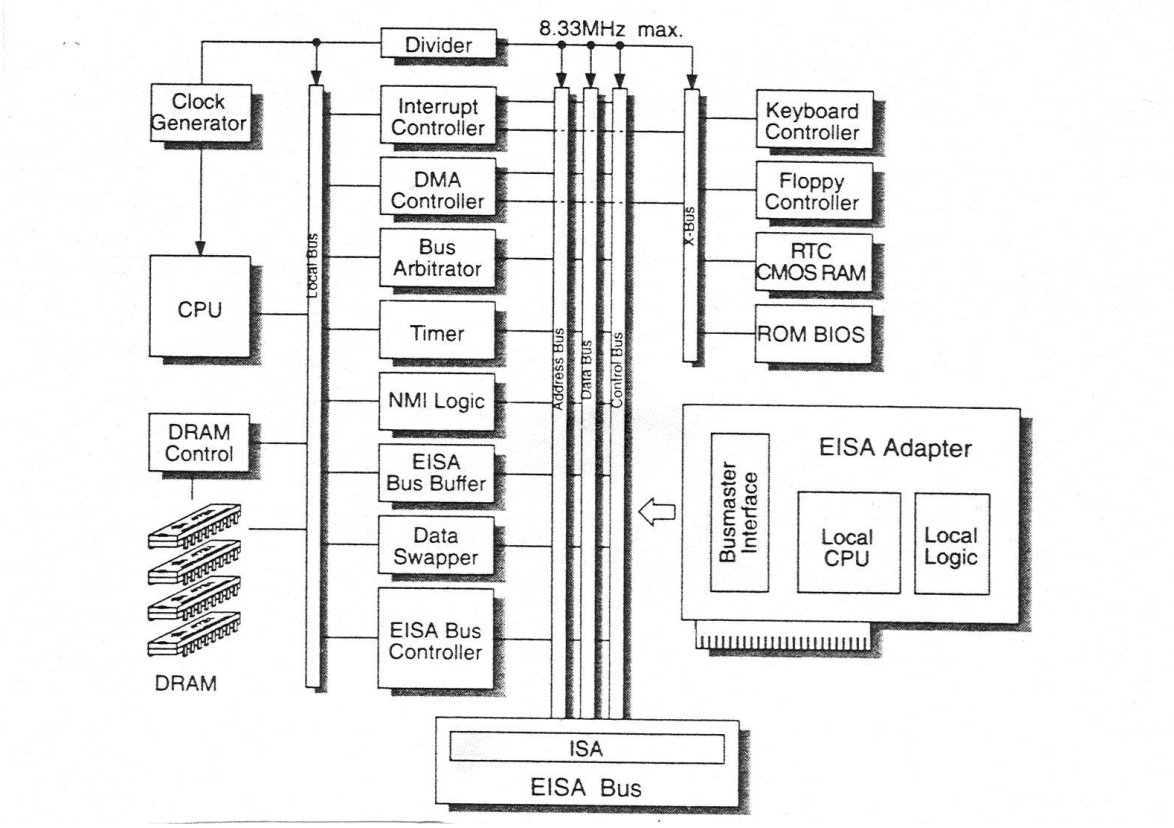


Figure 1.12: A controller and drives. The controller's microprocessor controls the components according to the microprogram in the ROM code. Data is transferred beween the drive and controller via an interface.


8.33MHz max.
Divider
Clock Generator
CPU
DRAM Control
DRAM
Local Bus
Interrupt Controller
DMA Controller
Bus Arbitrator
Timer
NMI Logic
EISA Bus Buffer
Data Swapper
EISA Bus Controller
Address Bus
Data Bus
Control Bus
X-Bus
Keyboard Controller
Floppy Controller
RTC CMOS RAM
ROM BIOS
EISA Adapter
Busmaster Interface
Local CPU
Local Logic
ISA
EISA Bus

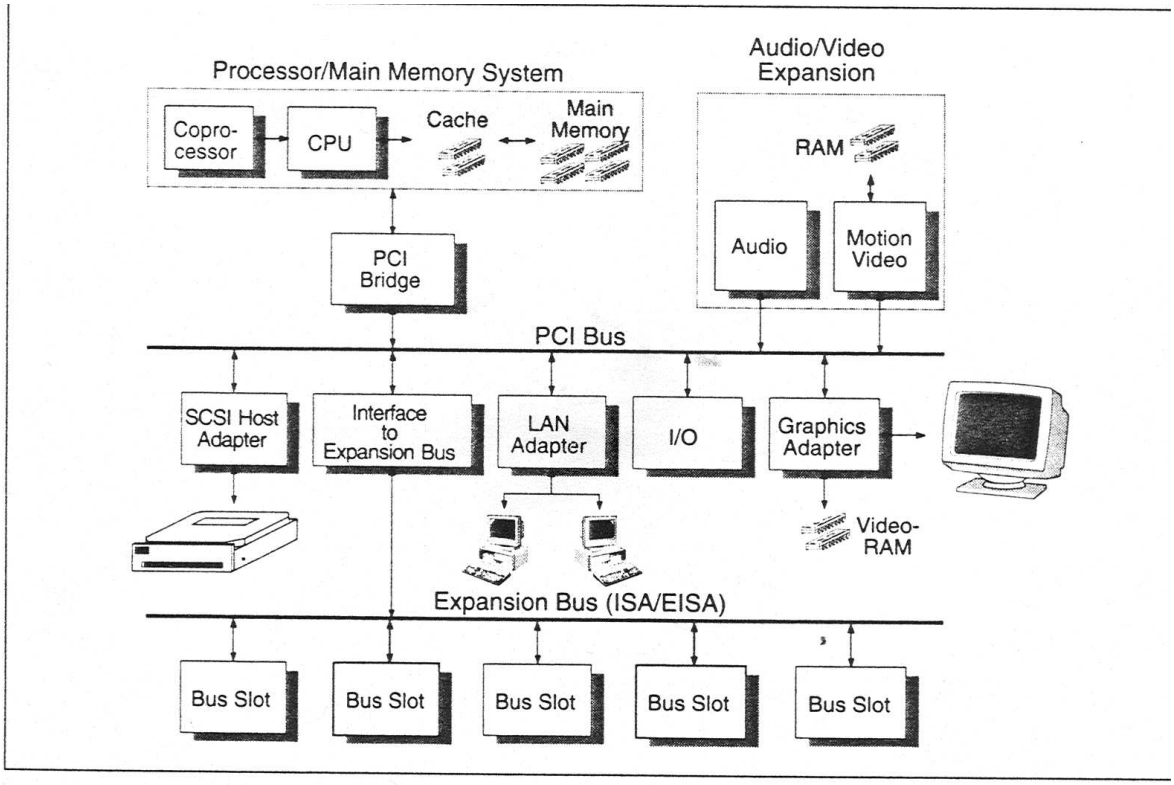
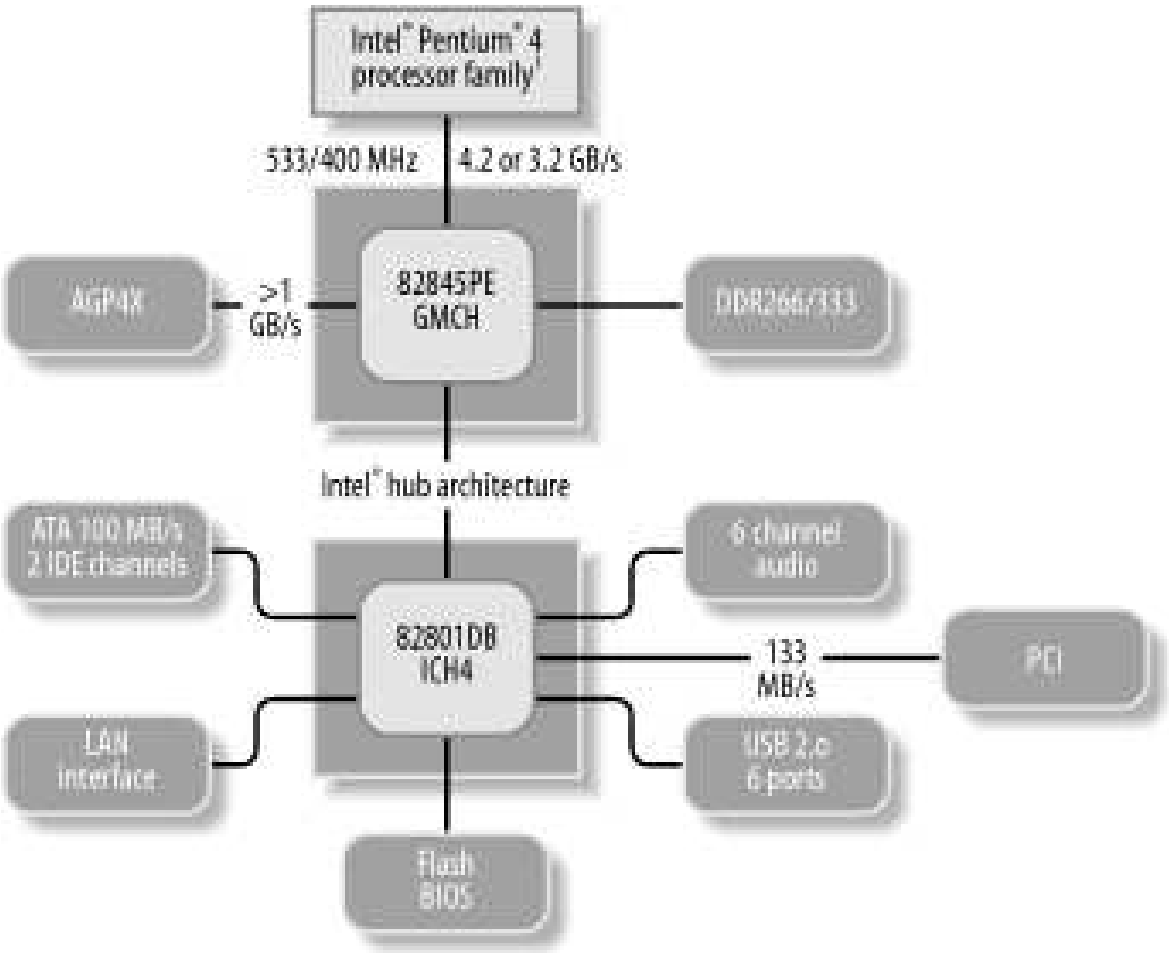


Figure 22.1: The PCI bus.


Intel® Pentium® 4 processor family*
533/400 MHz
4.2 or 3.2 GB/s
AGP4X
>1 GB/s
82845PE GMCH
DDR266/333
Intel® hub architecture
ATA 100 MB/s 2 IDE channels
6 channel audio
82801DB ICH4
133 MB/s
PCI
LAN interface
USB 2.0 6 ports
Flash BIOS

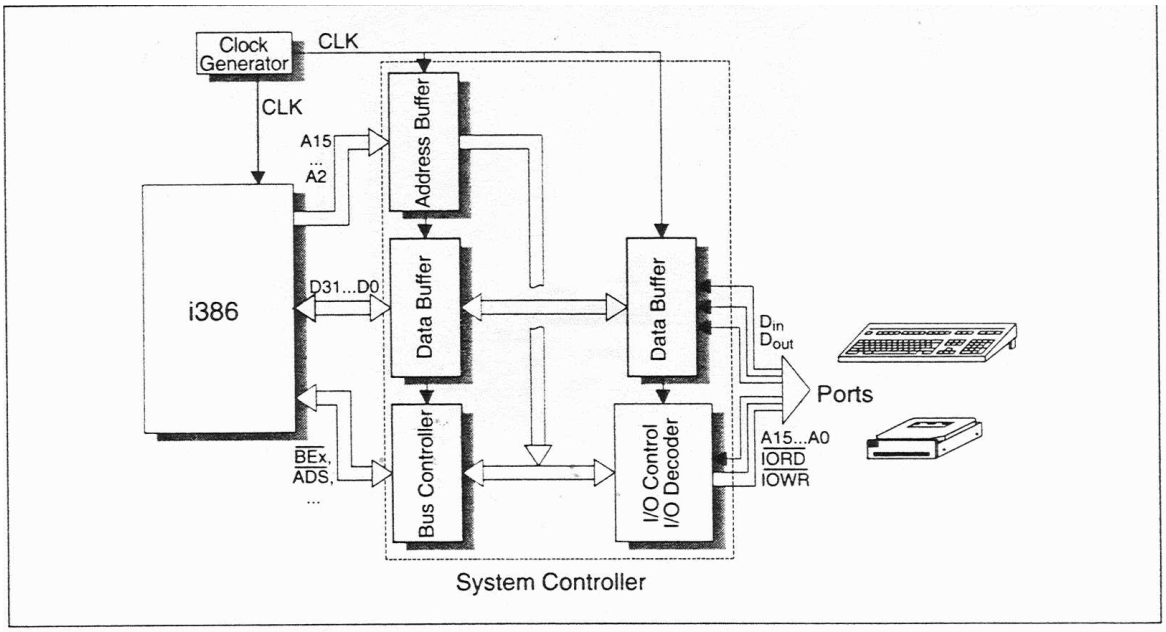
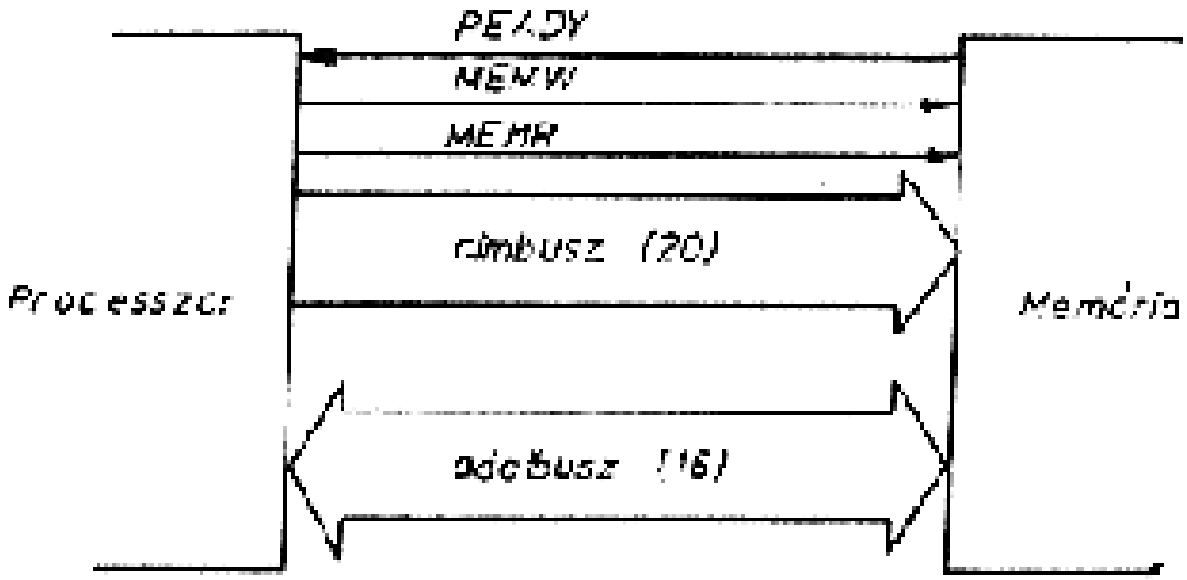
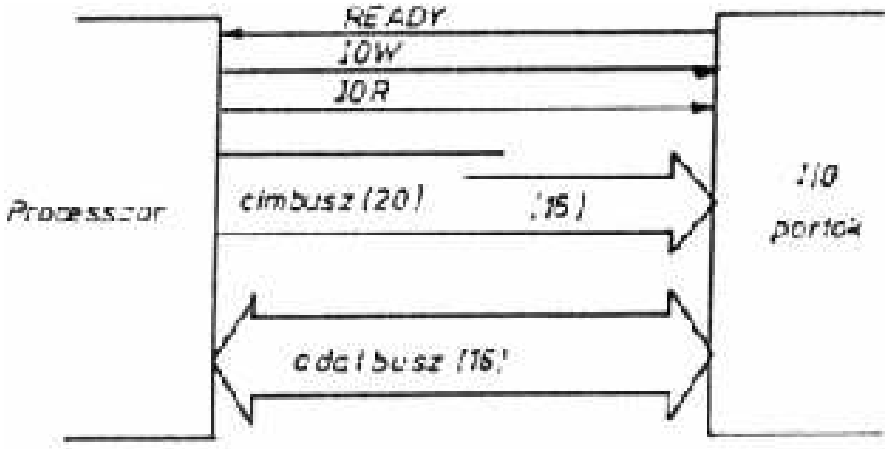


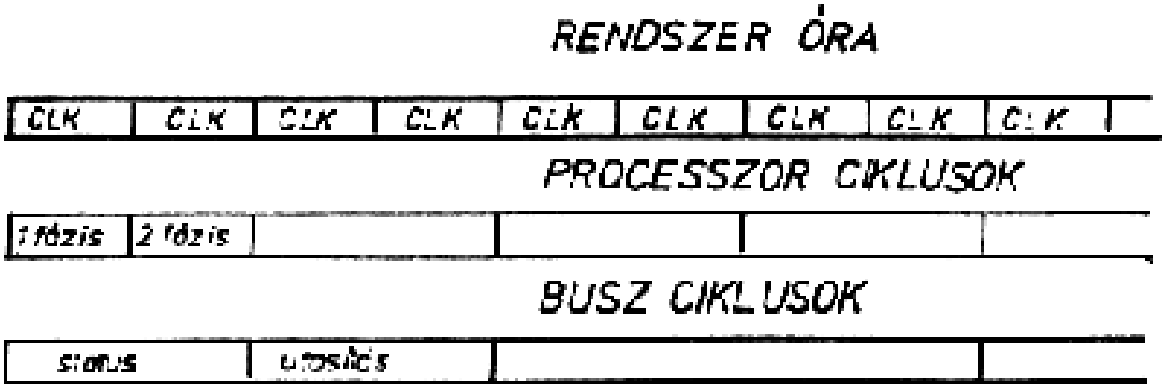
Figure 4.8: The path between processor and ports. Usually the processor does not access the I/O address space directly, but instead via a bus controller, as is the case for main memory, too. The bus controller generates the necessary control signals for the bus and various buffers for temporary storage and amplifying the data and address signals. These intermediate circuits are today integrated into one single system controller.



8.2.1. ábra



8.2.3. ábra


RENDSZER ÓRA
CLK
CLK
CLK
CLK
CLK
CLK
CLK
CLK
CLK
PROCESSZOR CIKLUSOK
1 fázis
2 fázis
BUSZ CIKLUSOK
START

8.3.1. ábra

Interrupt

8.1.3. ábra

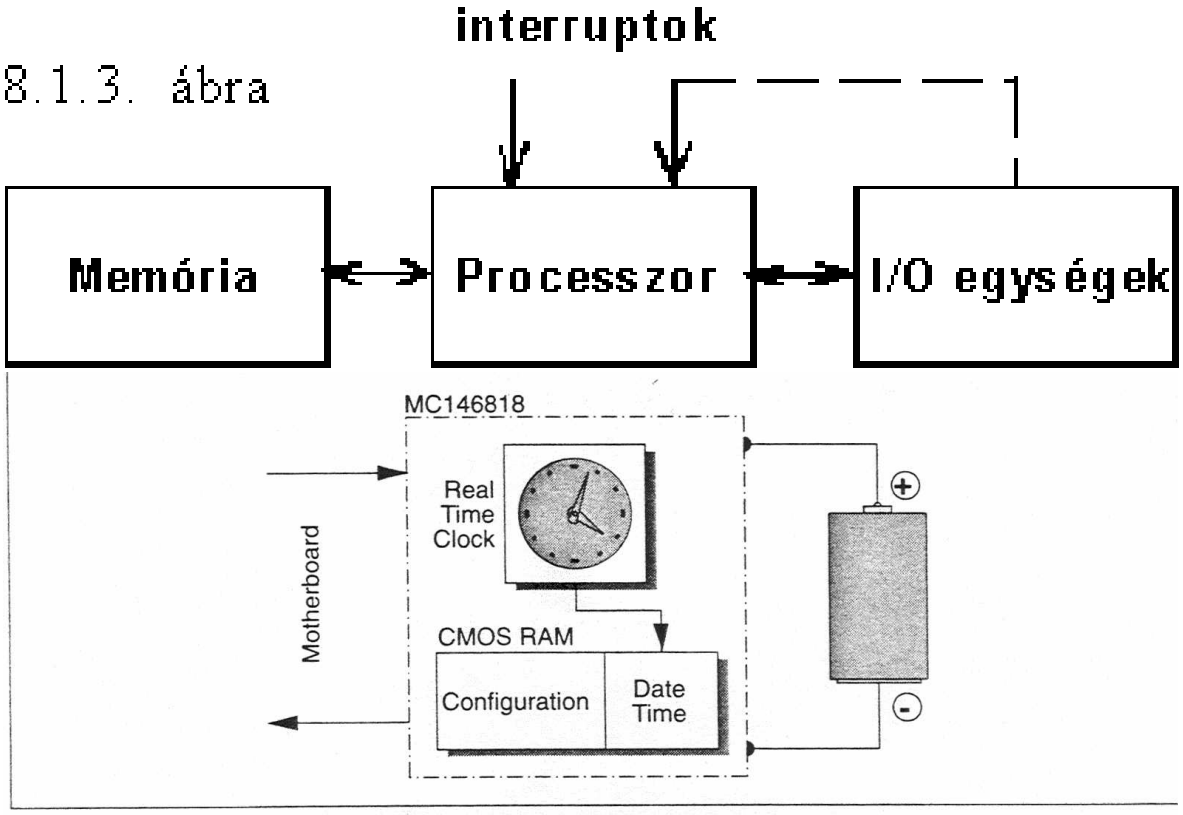


Figure 1.21: CMOS RAM and real-time clock. The PC has an MC146818 chip which has a real-time clock and a battery buffered CMOS RAM in which to store the configuration data.

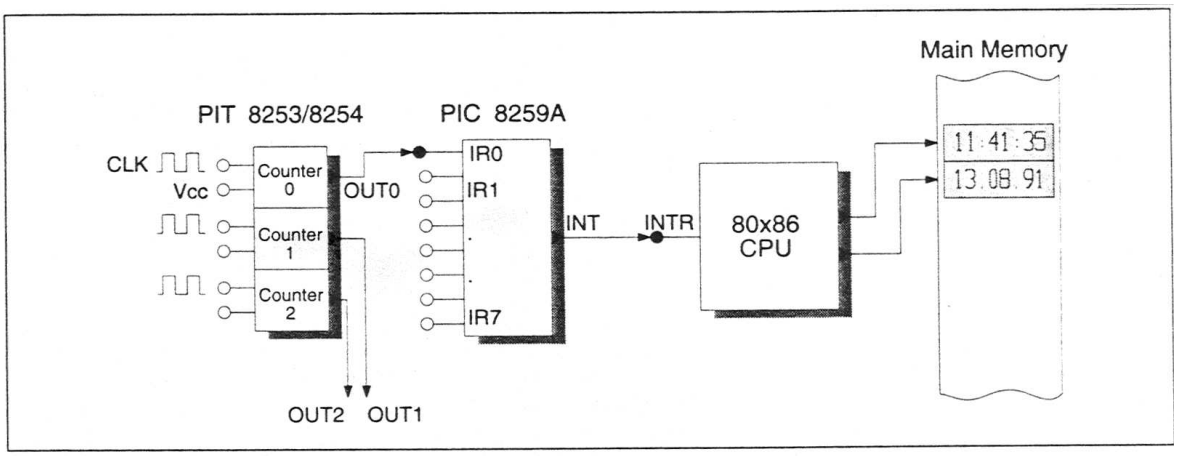


Figure 24.9: Scheme of the internal system clock. The counter 0 periodically issues a hardware interrupt via IRQ0 so that the CPU can update the DOS system clock.

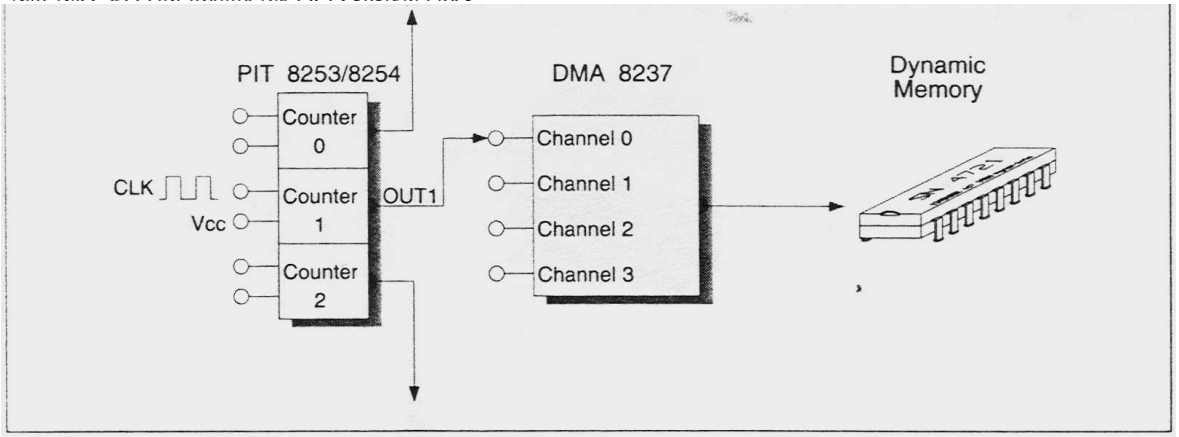
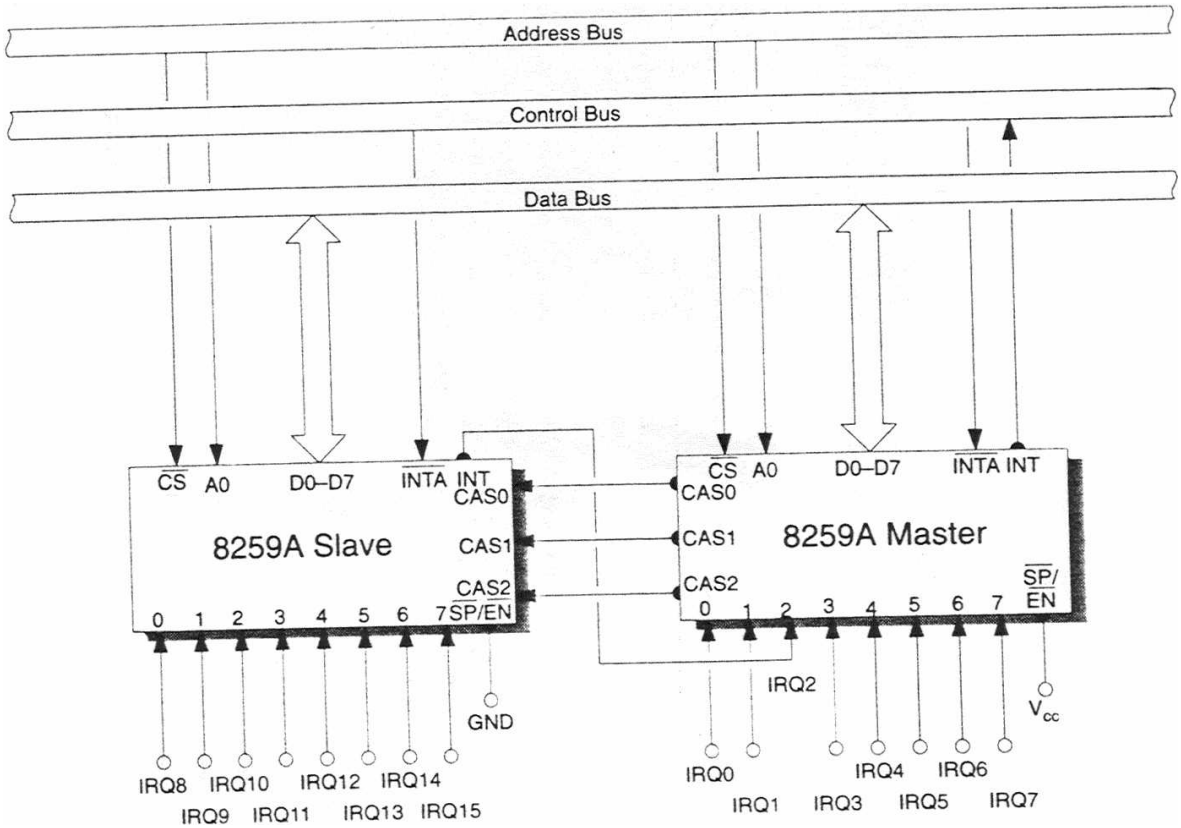
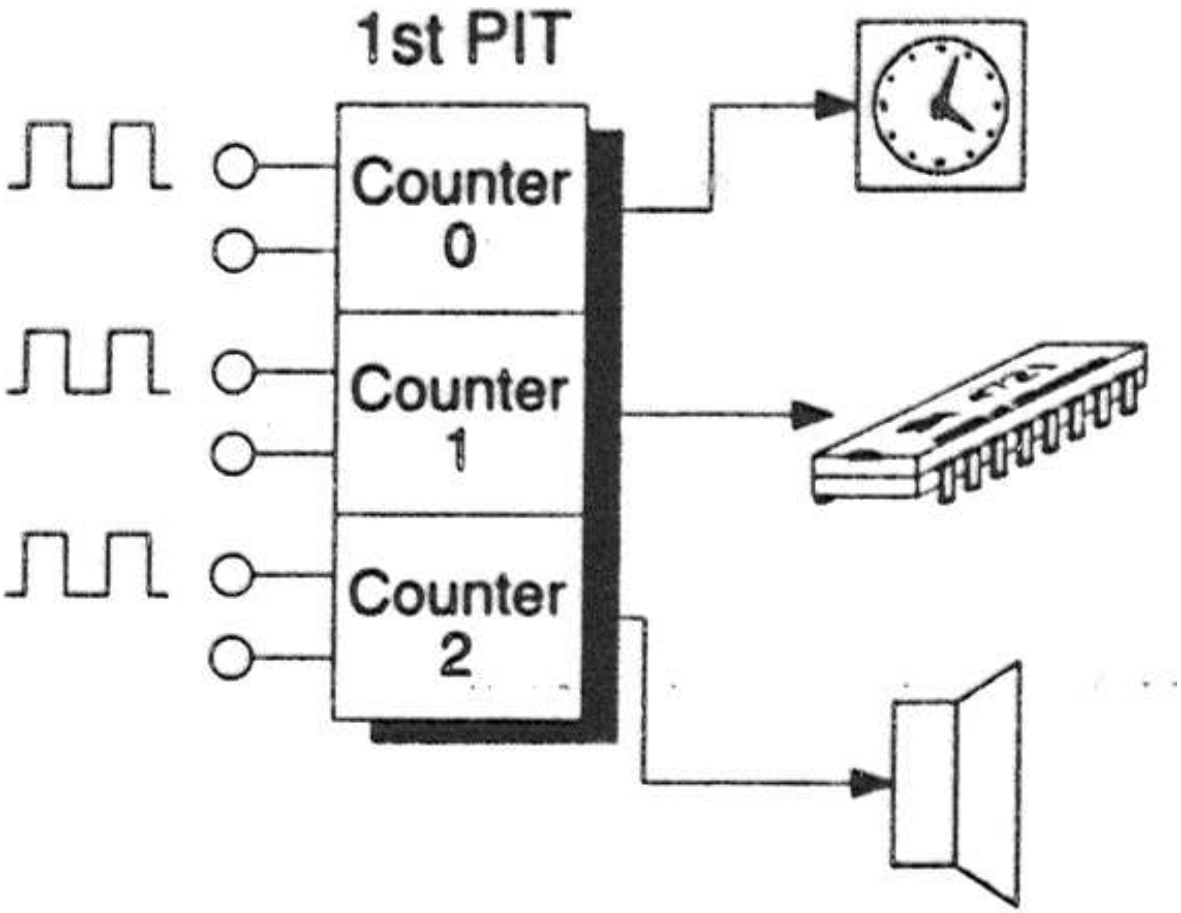
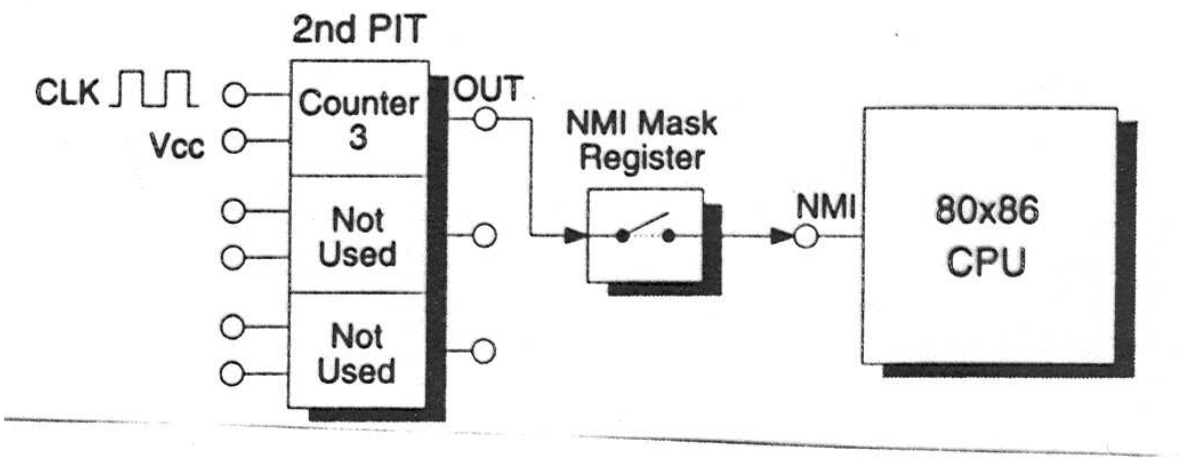


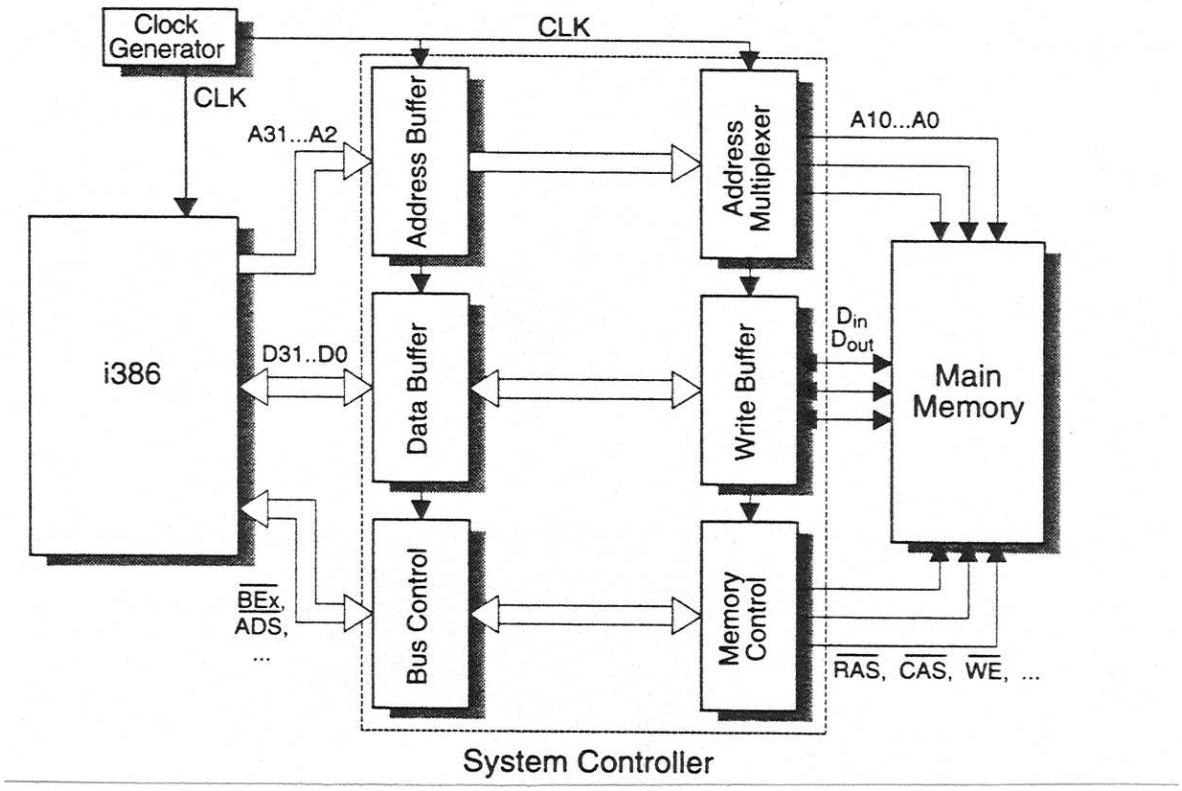
Figure 24.10: Connection of timer and DMA chip for the memory refresh. The counter periodically activates channel 0 of the 8237A DMA chip, which carries out a dummy read cycle to refresh the DRAM memory.

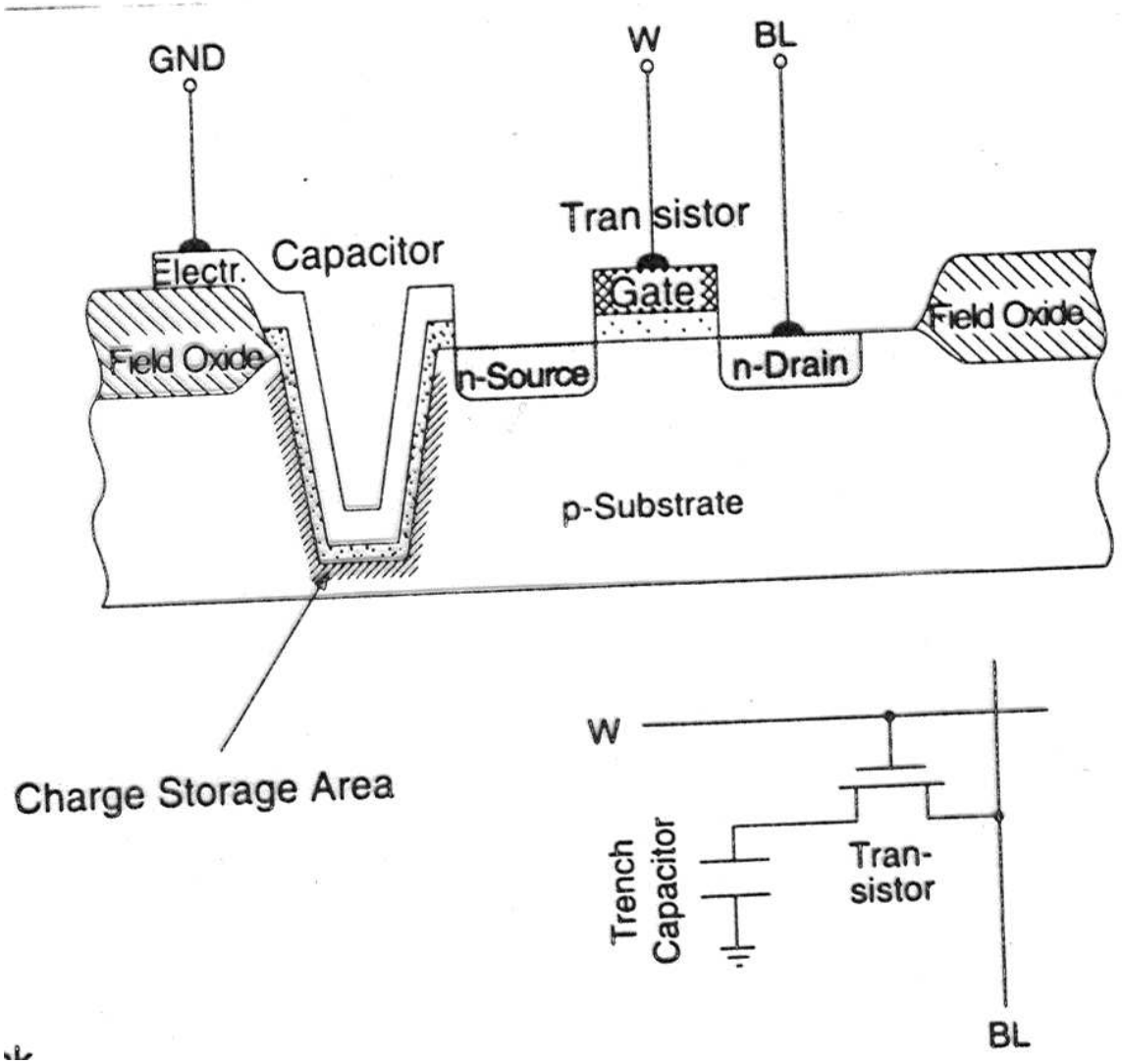

Address Bus
Control Bus
Data Bus
CS A0 D0–D7 INTA INT
CAS0
CAS1
CAS2
8259A Slave
SP/EN
0 1 2 3 4 5 6 7
GND
IRQ8 IRQ10 IRQ12 IRQ14
IRQ9 IRQ11 IRQ13 IRQ15
CS A0 D0–D7 INTA INT
CAS0
CAS1
CAS2
8259A Master
SP/EN
0 1 2 3 4 5 6 7
IRQ2
Vcc
IRQ0 IRQ4 IRQ6
IRQ1 IRQ3 IRQ5 IRQ7

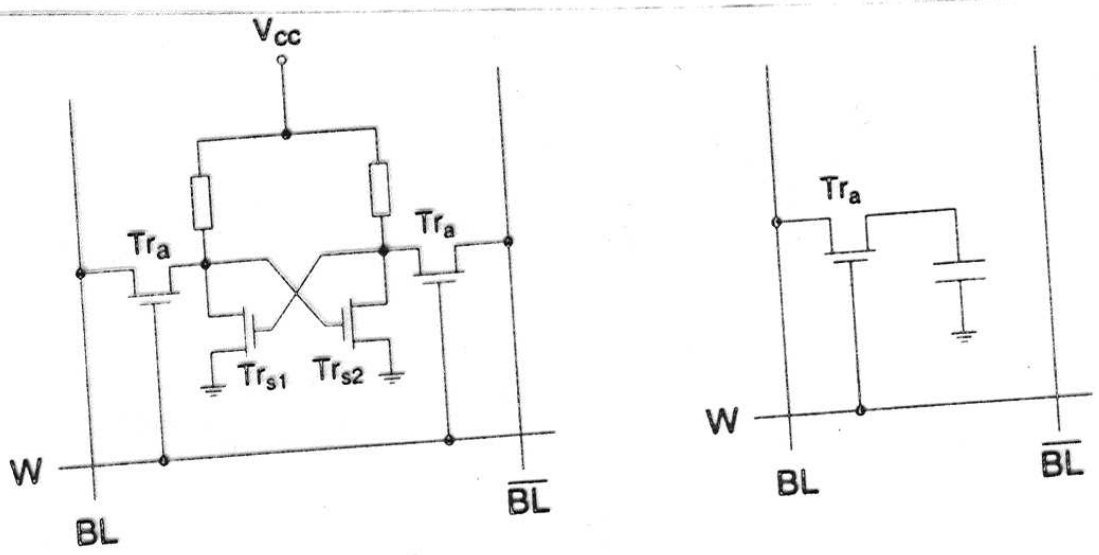

1st PIT
Counter 0
Counter 1
Counter 2

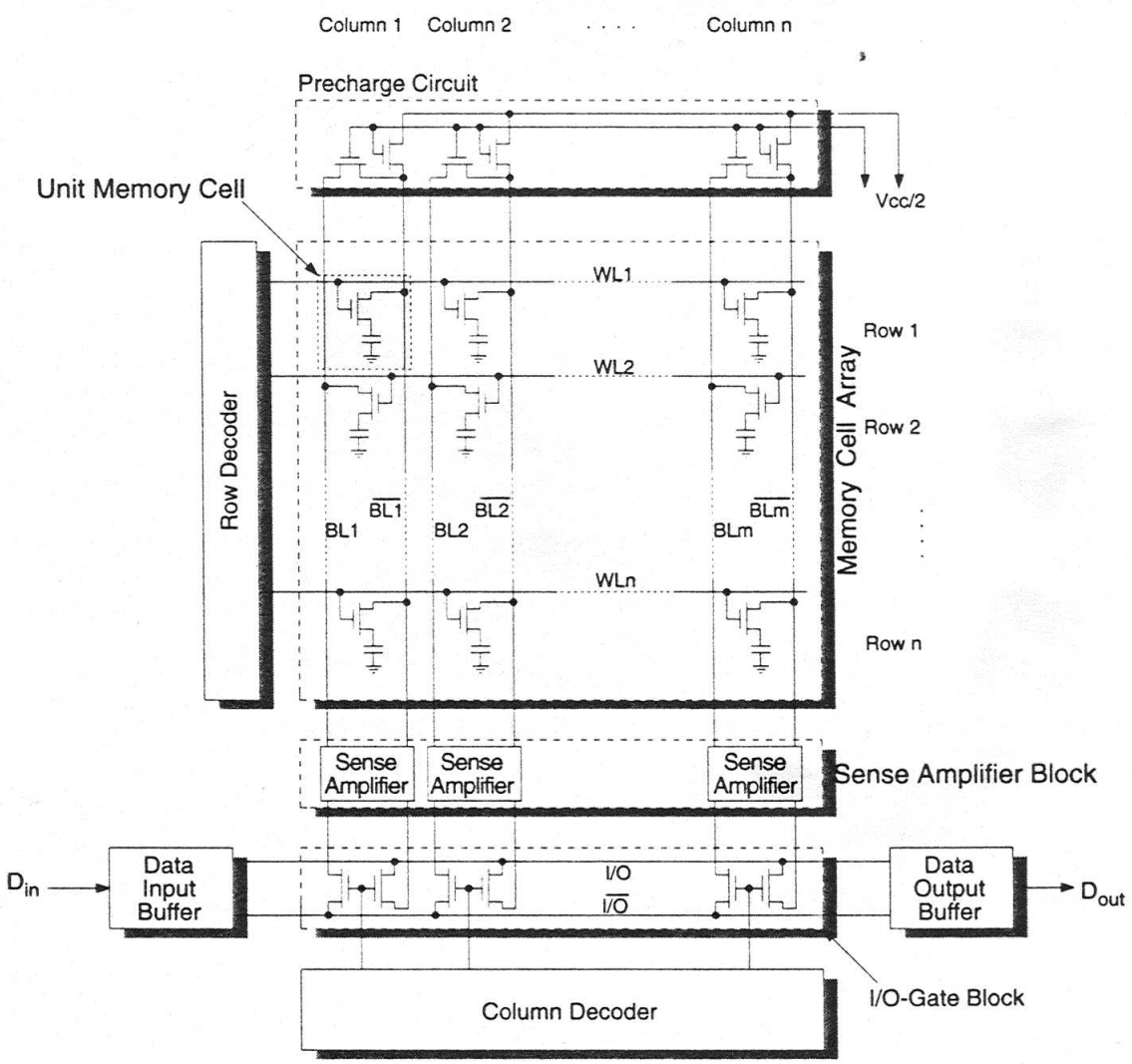

2nd PIT
CLK
Vcc
Counter 3
Not Used
Not Used
OUT
NMI Mask Register
NMI
80x86 CPU

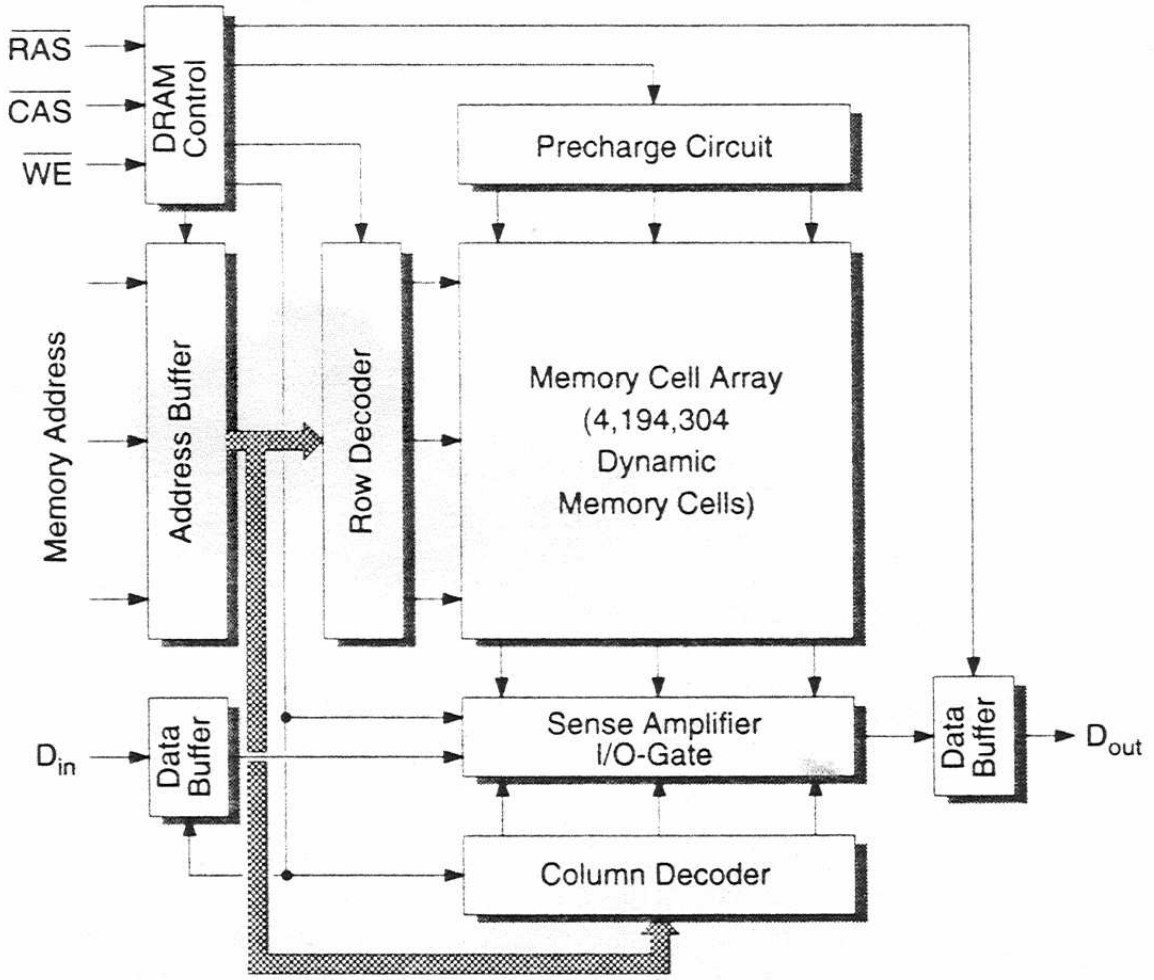
Memória

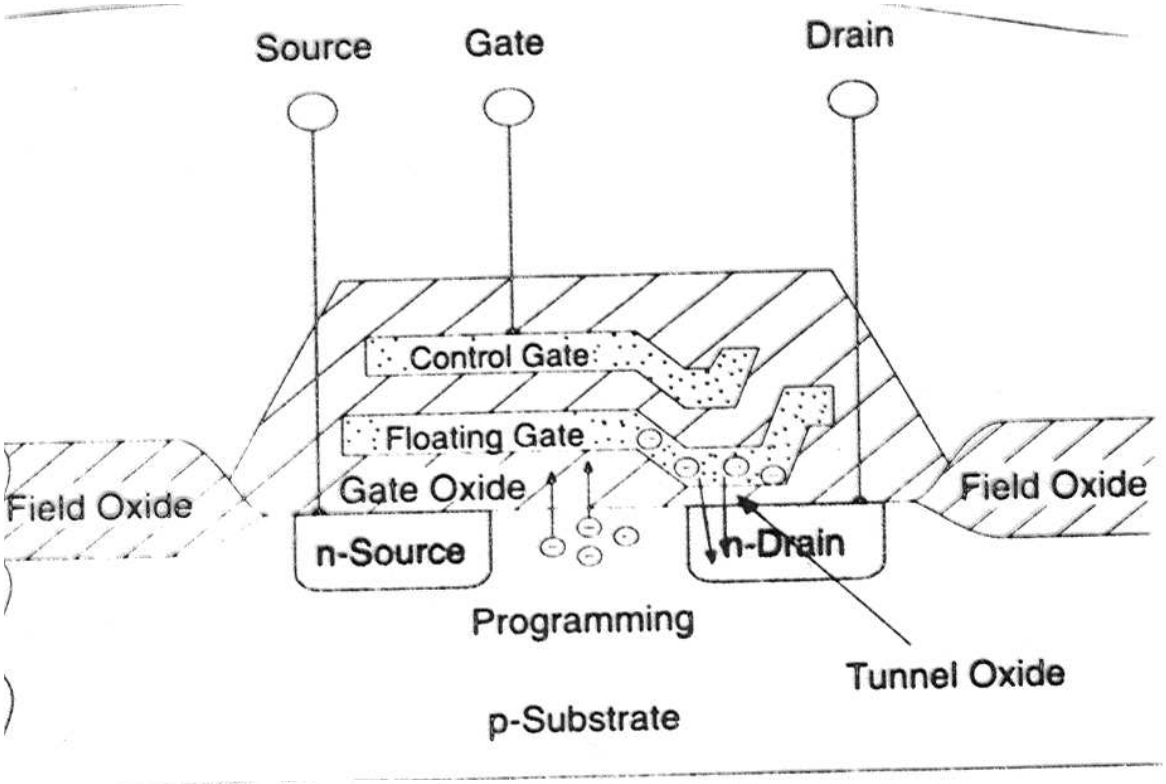

Clock Generator
CLK
CLK
A31...A2
Address Buffer
Address Multiplexer
A10...A0
i386
D31..D0
Data Buffer
Write Buffer
Din
Dout
Main Memory
BEx,
ADS,
...
Bus Control
Memory Control
RAS, CAS, WE, ...
System Controller

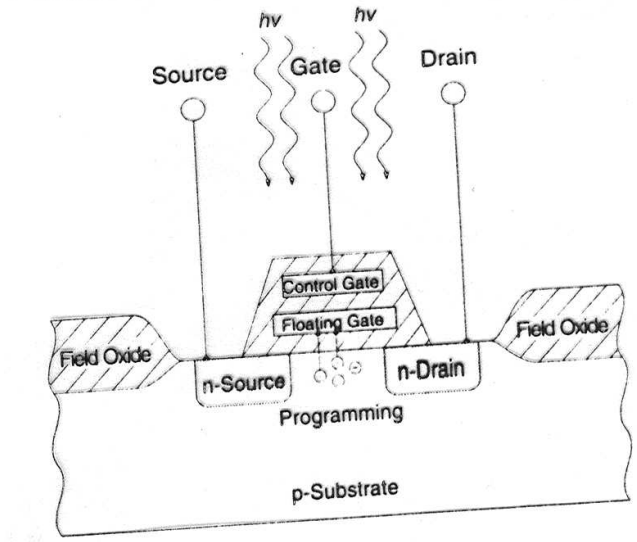

GND
W
BL
Tran sistor
Capacitor
Electr.
Gate
Field Oxide
Field Oxide
n-Source
n-Drain
p-Substrate
Charge Storage Area
W
Trench Capacitor
Tran-sistor
BL

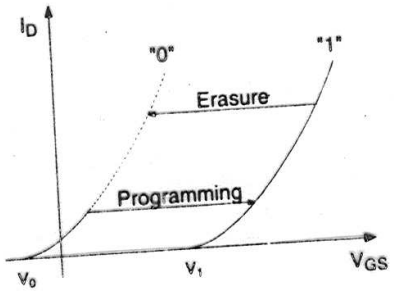

Vcc
Tra
Tra
Trs1
Trs2
W
BL
BL
Tra
W
BL
BL

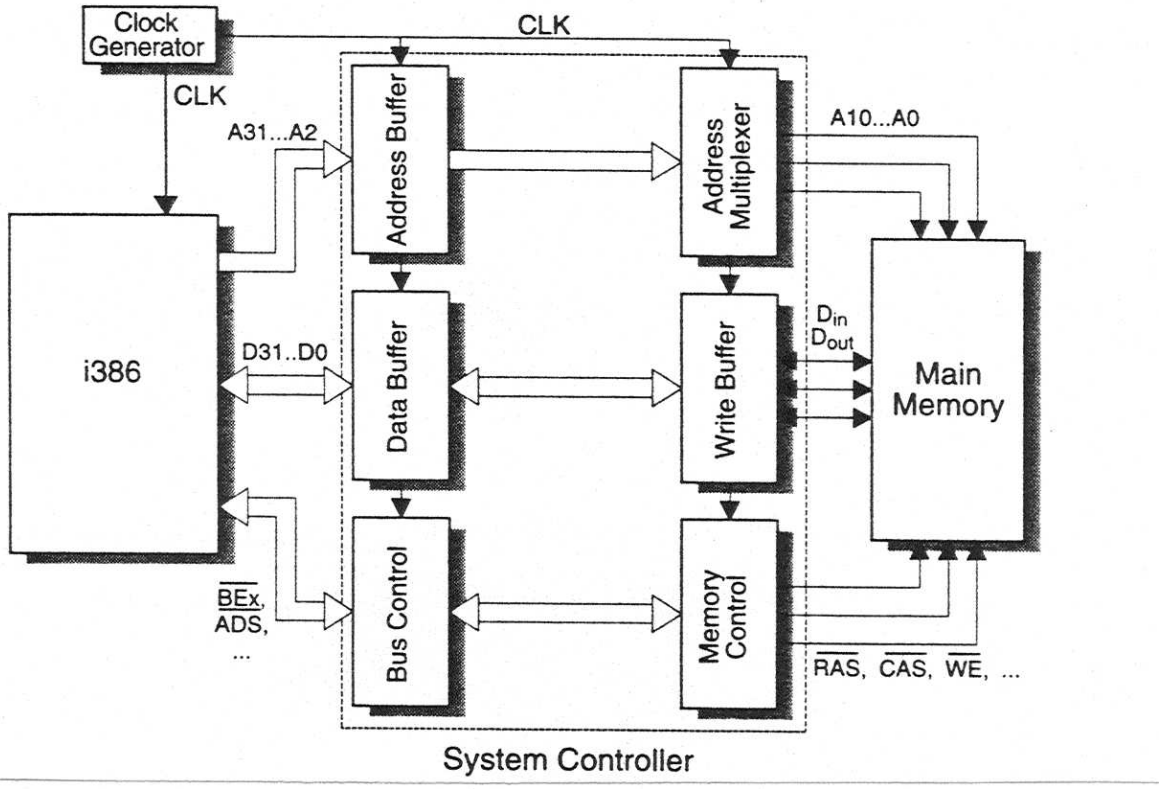

Column 1
Column 2
Column n
Precharge Circuit
Unit Memory Cell
Vcc/2
WL1
WL2
WLn
Row 1
Row 2
Row n
Row Decoder
Memory Cell Array
BL1
BL2
BLm
Sense Amplifier
Sense Amplifier
Sense Amplifier
Sense Amplifier Block
Din
Data Input Buffer
I/O
Data Output Buffer
Dout
Column Decoder
I/O-Gate Block


RAS
CAS
WE
DRAM Control
Precharge Circuit
Memory Address
Address Buffer
Row Decoder
Memory Cell Array
(4,194,304
Dynamic
Memory Cells)
Data Buffer
Sense Amplifier
I/O-Gate
Data Buffer
Din
Dout
Column Decoder


Source
Gate
Drain
Control Gate
Floating Gate
Gate Oxide
Field Oxide
Field Oxide
n-Source
n-Drain
Programming
Tunnel Oxide
p-Substrate


hv
hv
Source
Gate
Drain
Control Gate
Floating Gate
Field Oxide
Field Oxide
n-Source
n-Drain
Programming
p-Substrate


I_D
"0"
"1"
Erasure
Programming
V_0
V_1
V_{GS}


Clock Generator
CLK
CLK
A31...A2
Address Buffer
Address Multiplexer
A10...A0
i386
D31..D0
Data Buffer
Write Buffer
Din
Dout
Main Memory
BEx,
ADS,
...
Bus Control
Memory Control
RAS, CAS, WE, ...
System Controller

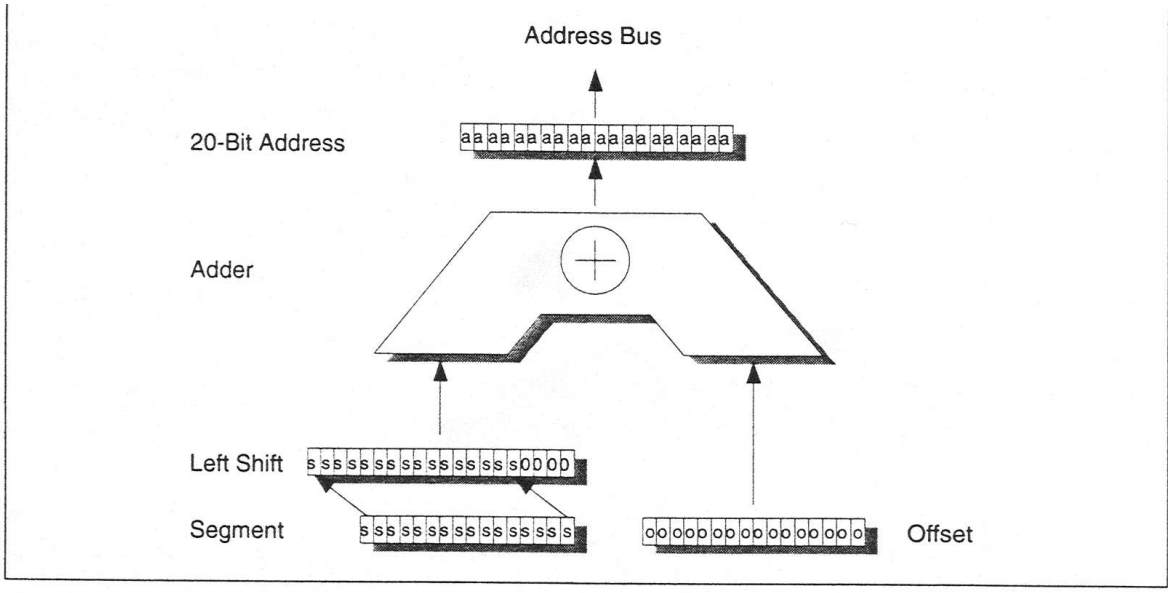


Figure 2.7: Combination of segment address and offset in real mode. In real mode the addressing unit shifts the segment register value left by four bits, thus multiplying the segment value by 16, and adds the offset. The result is a 20-bit address.

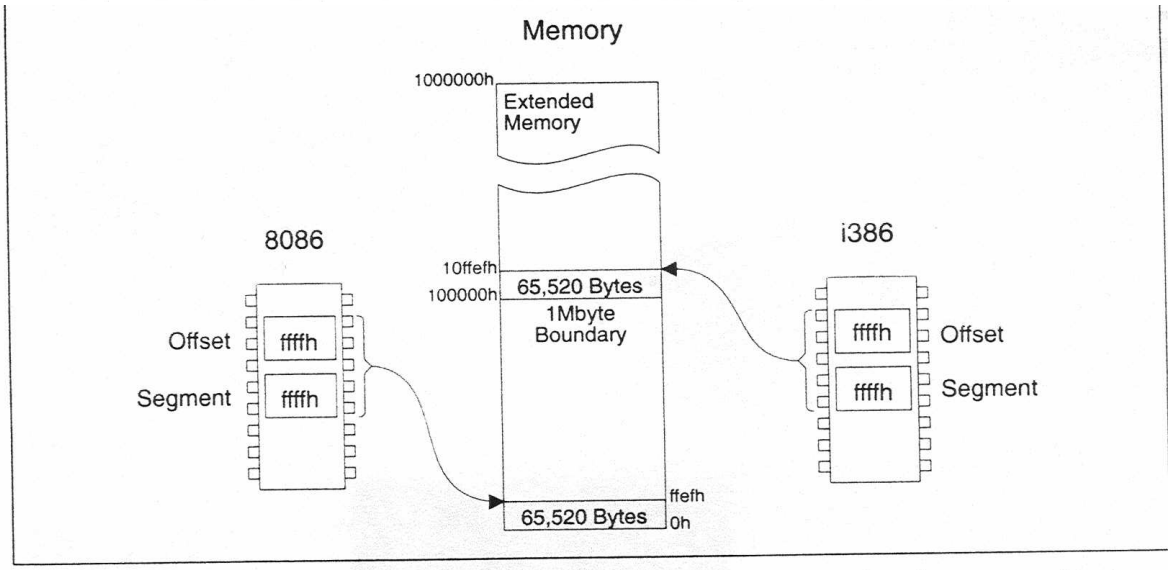


Figure 3.2: Breakthrough of the 1 Mbyte barrier in real mode. In real mode, when the value of a segment register is multiplied by 16 and the offset is added, the result may be above 1 Mbyte. Because of the 32 address lines of the i386

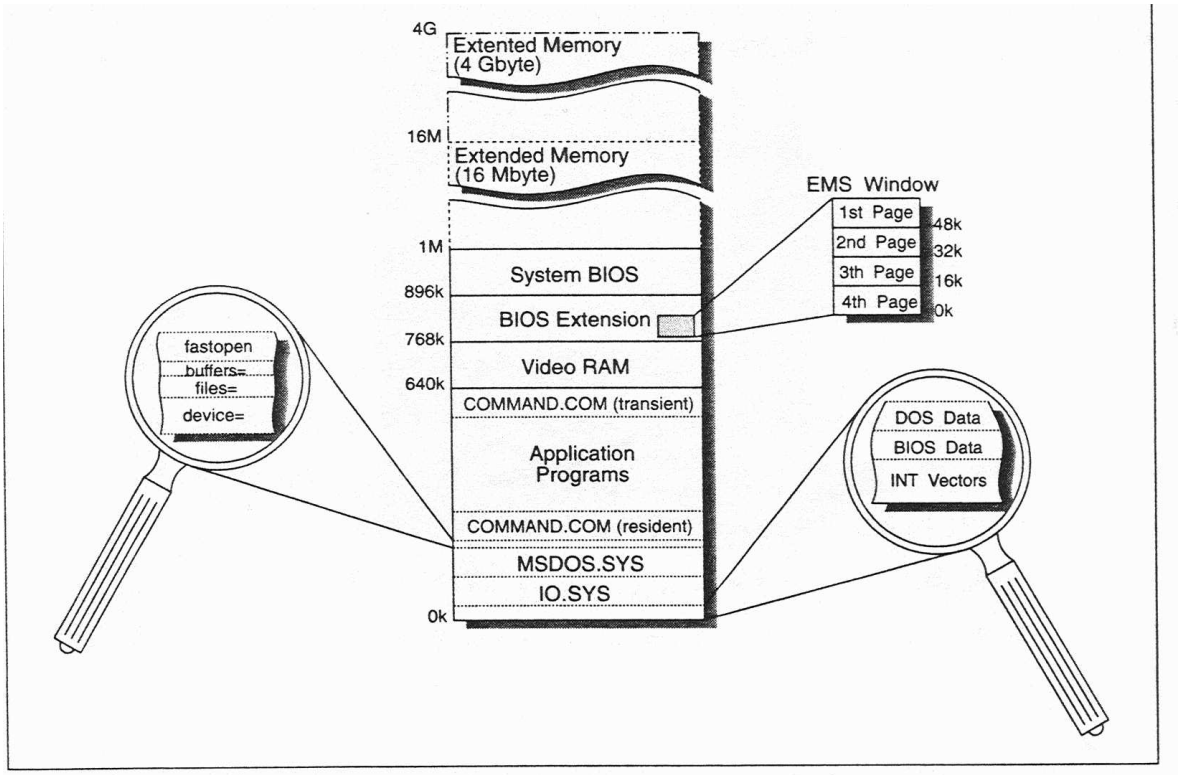
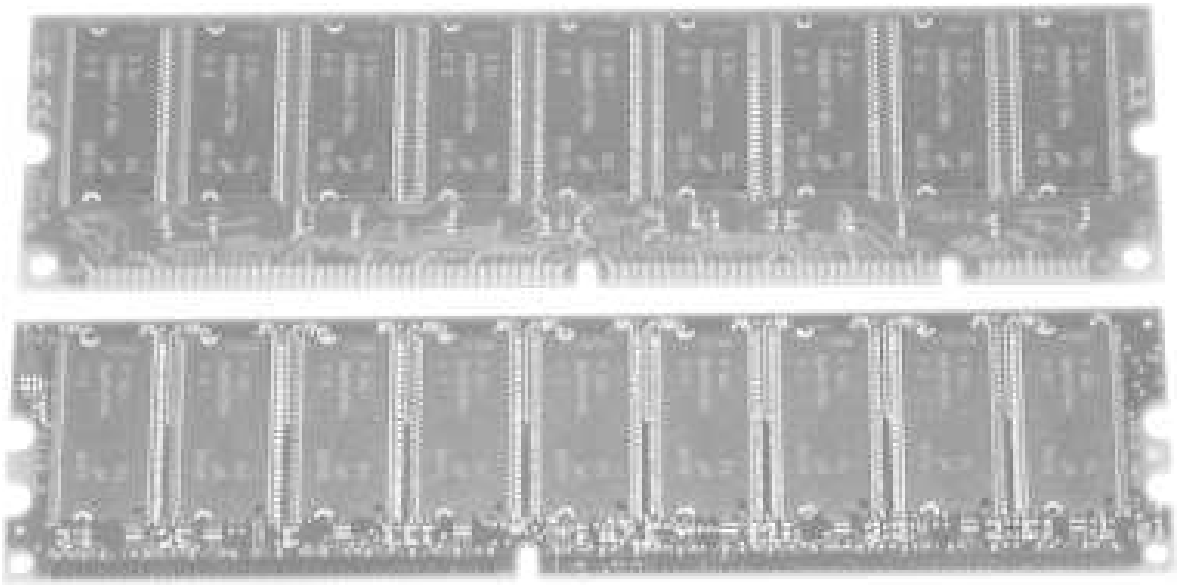
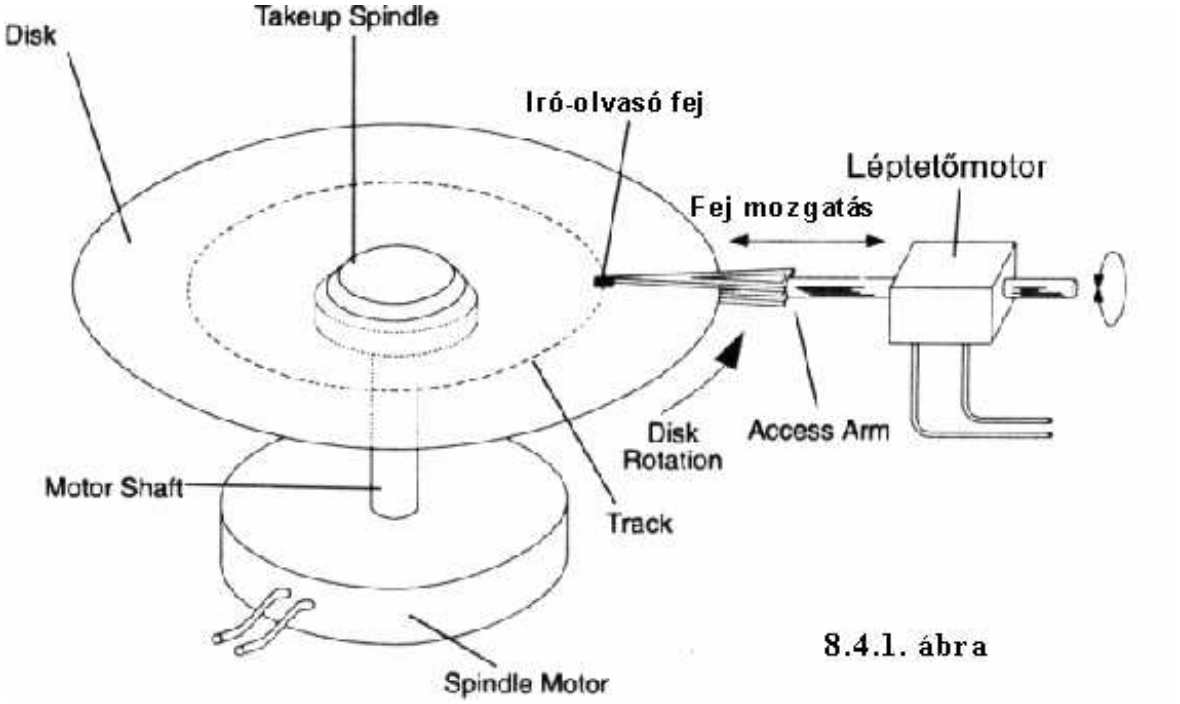


Figure 1.28: DOS memory organization. With DOS the first 640 kbytes are reserved for the operating system and application programs. Above the first 640 kbytes there is the video RAM, and starting from 768 kbytes there follow various (and optional) BIOS extensions. Above 1 Mbyte extended memory starts, which can be up to 4 Gbyte on an i386, i486 or Pentium.



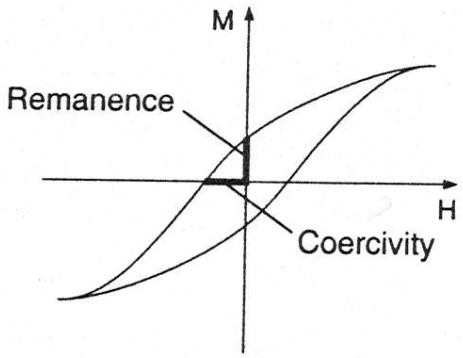
ECC - paritásvizsgálat (kozmikus sugárzás!) > 512MB

Diszk

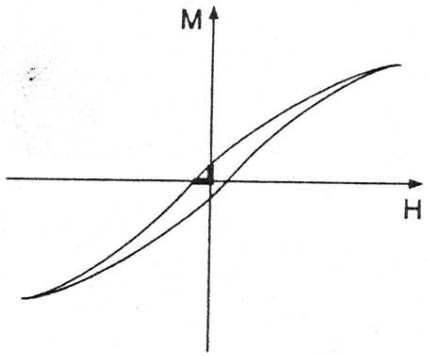


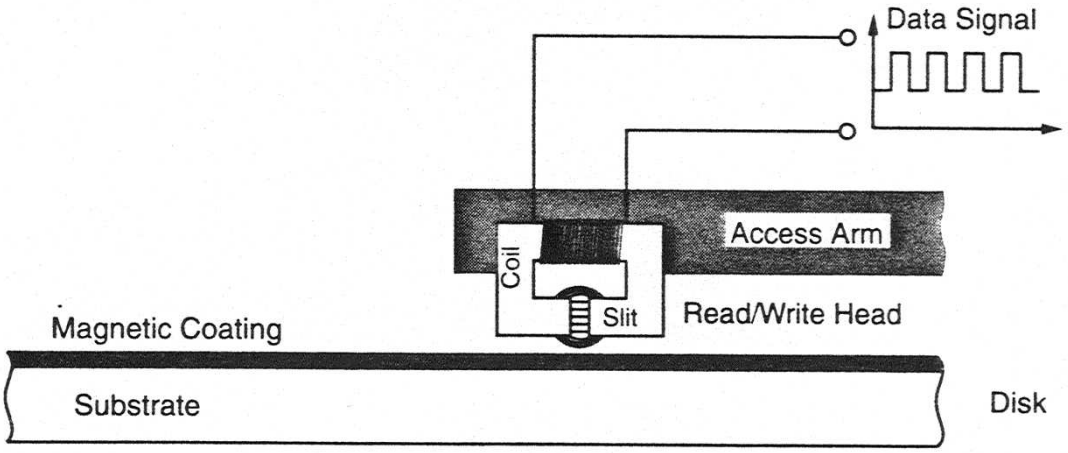
8.4.1. ábra

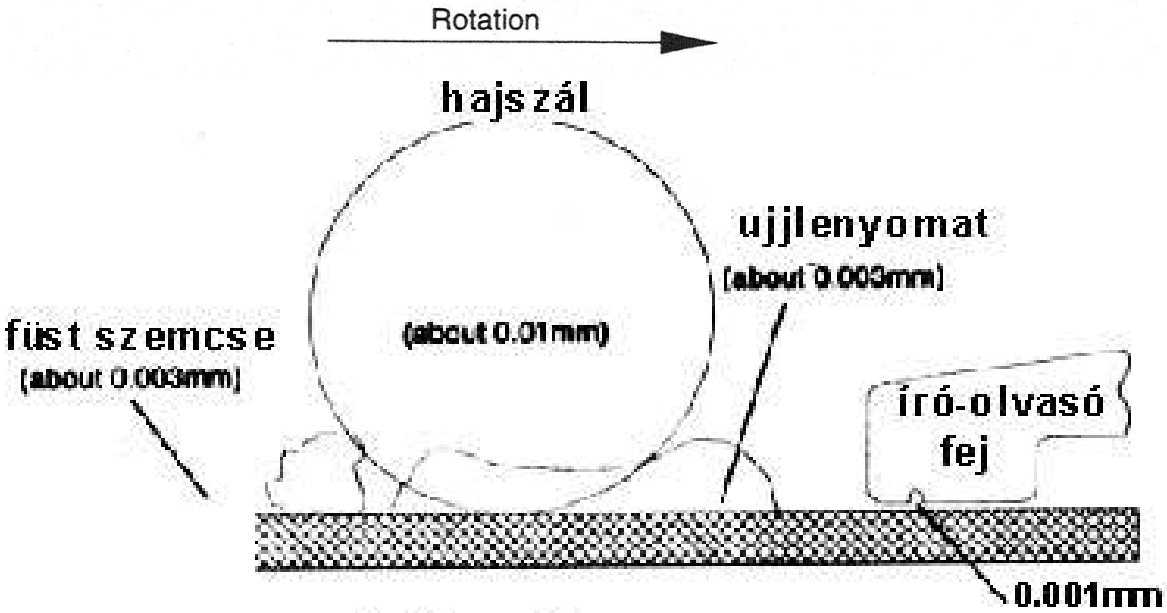
Ferromagnetic Hard Material



Ferromagnetic Soft Material




Data Signal
Access Arm
Coil
Slit
Read/Write Head
Magnetic Coating
Substrate
Disk


Rotation
hajszál
ujjlenyomat
(about 0.003mm)
(about 0.01mm)
(about 0.003mm)
író-olvasó
fej
0.001mm

8.4.2. ábra

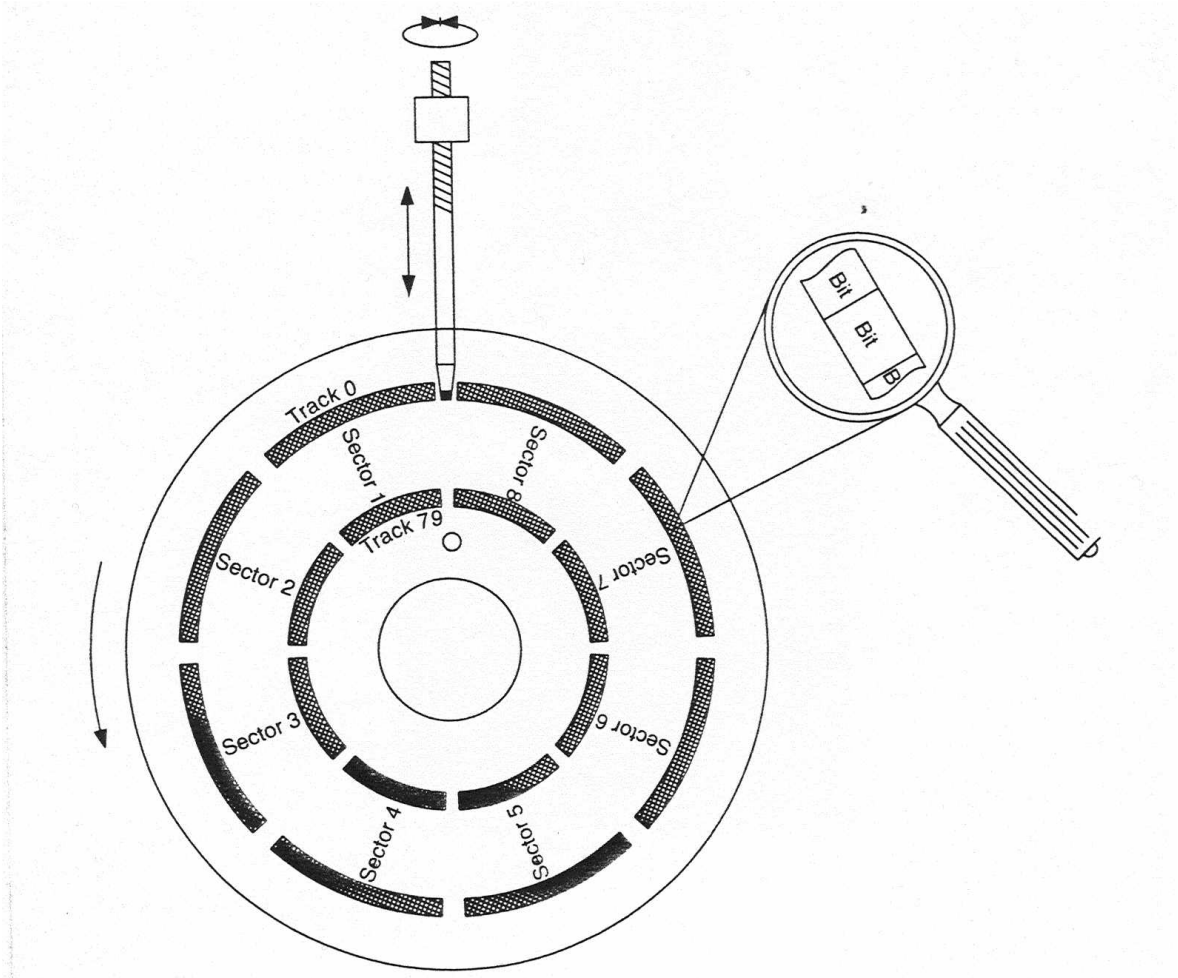


Figure 27.6: Tracks, cylinders and sectors. Every floppy disk is organized into tracks, which in turn are divided into sectors. Within one sector the bit is the smallest data unit.

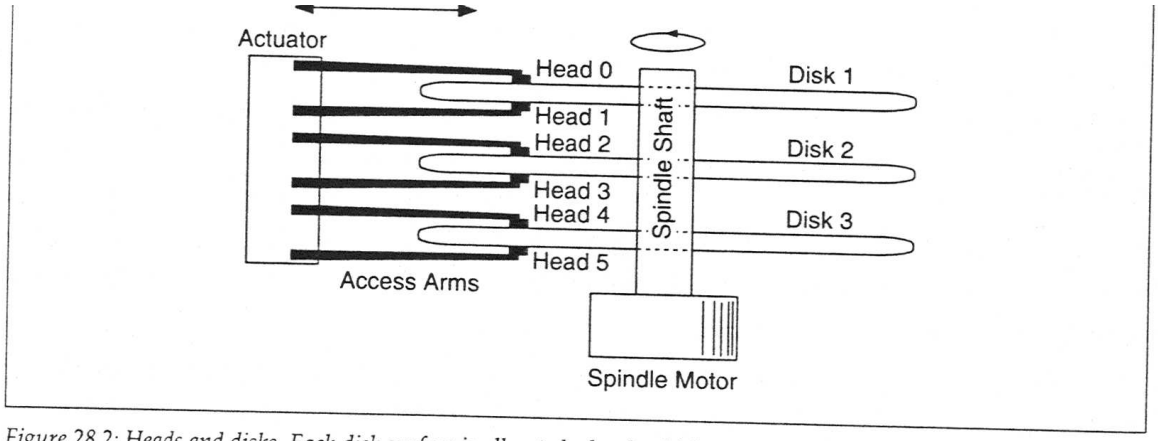


Figure 28.2: Heads and disks. Each disk surface is allocated a head, which is fixed to the end of an access arm. All arms and heads are moved in common and simultaneously by a single actuator.

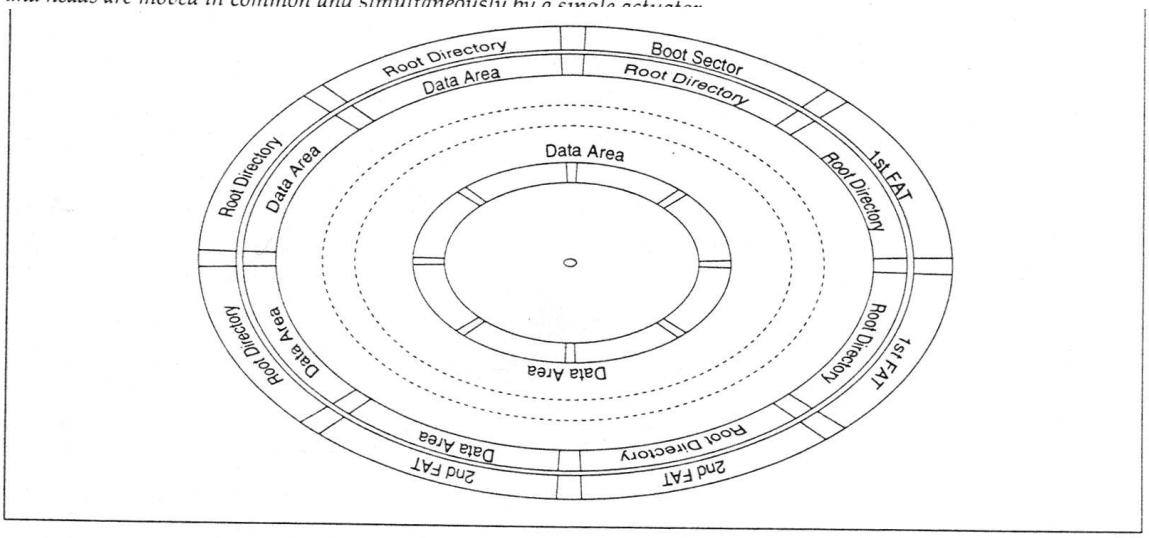
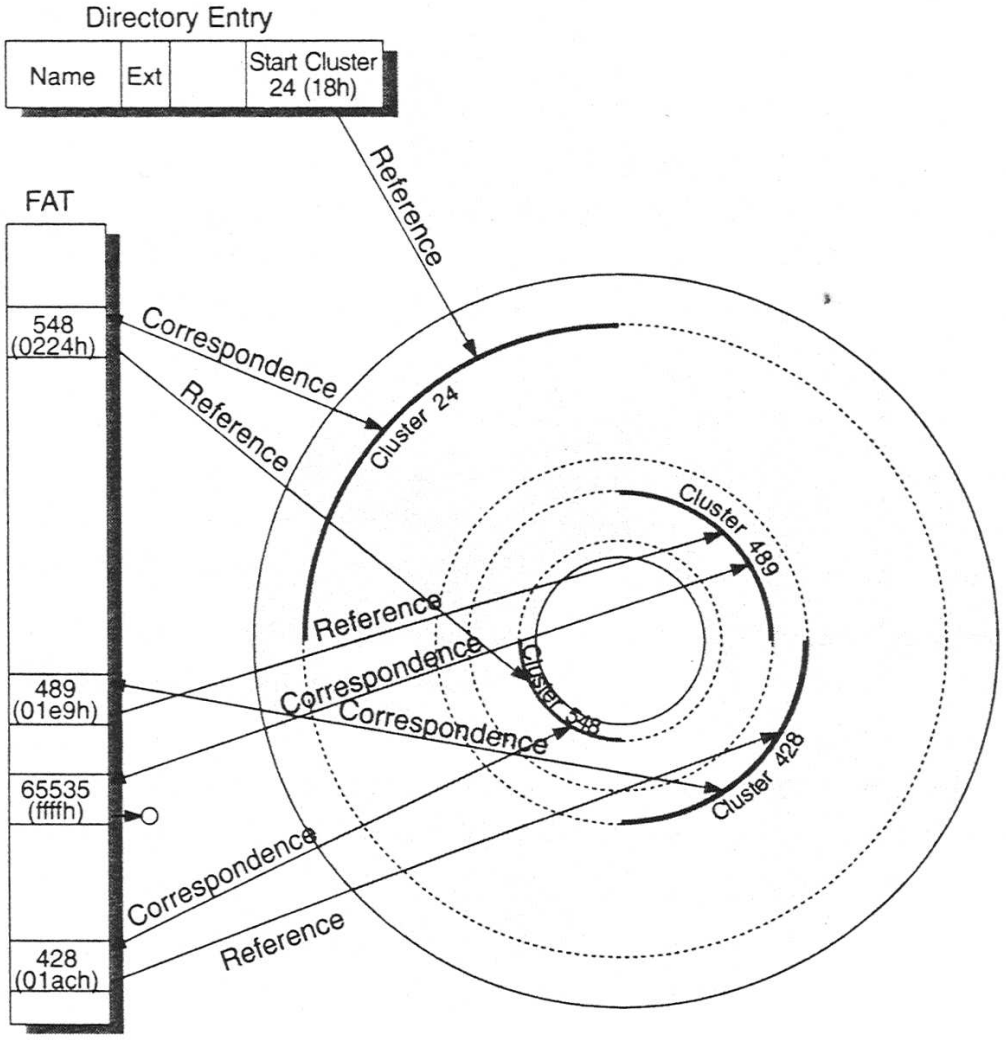


Figure 27.10: Arrangement of boot sector, FATs, root directory, subdirectories and files. On a floppy disk, from the outside to the inside are located the boot sector, the two FAT copies and the root directory. These are followed by the data area, which fills the floppy disk up to the innermost cylinder.



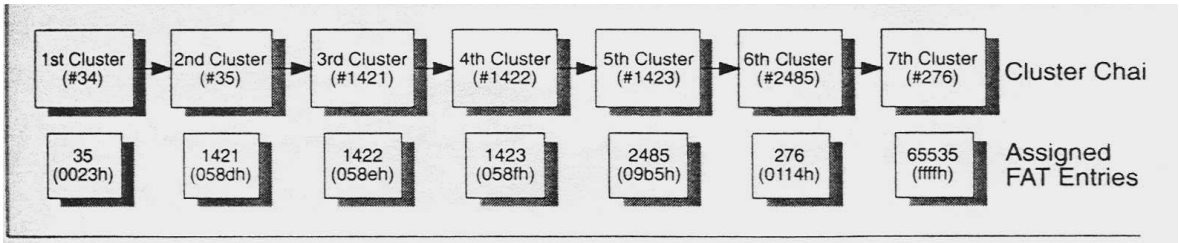
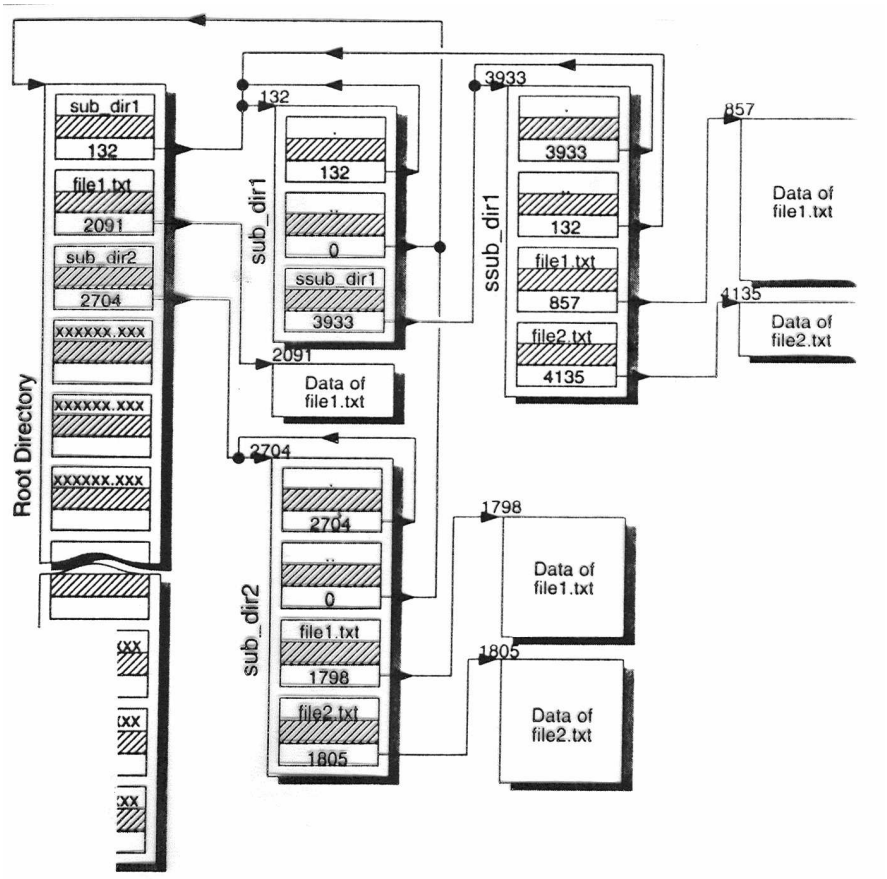
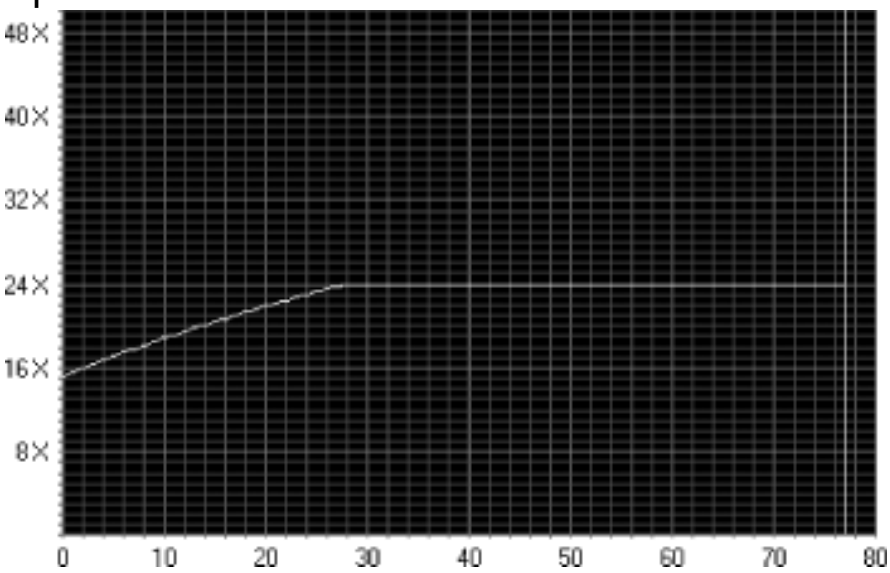


Figure 27.15: Cluster chain.


Root Directory
sub_dir1
132
file1.txt
2091
sub_dir2
2704
xxxxxx.xxx
xxxxxx.xxx
xxxxxx.xxx
xx
xx
xx
132
sub_dir1
.
132
..
0
ssub_dir1
3933
2091
Data of file1.txt
2704
sub_dir2
.
2704
..
0
file1.txt
1798
file2.txt
1805
1798
Data of file1.txt
1805
Data of file2.txt
3933
ssub_dir1
.
3933
..
132
file1.txt
857
file2.txt
4135
857
Data of file1.txt
4135
Data of file2.txt

CD/DVD

Spirál



Videó kártya

	EGA		VGA		SVGA	
	karakter	grafika	karakter	grafika	karakter	grafika
felbontás (pixel)	640*350	640*350	640*480	640*480	1288*960	1280*1024
video szegmens	B800	A000	B800	A000	B800	A000
video RAM (kbyte)	64 - 256	64 - 256	256	256	>= 1000	>= 1000
karakter mátrix	8*14,8*8	8*14,8*8	9*16	9*16	9*16	9*16
színek száma	16 64-ből	16 64-ből	256	256	256	256, > 1m
monitor vezérlés	digitális	digitális	analóg	analóg	analóg	analóg
vízsz. frekvencia (kHz)	15.7-21.8	15.7-21.8	31.5	31.5	< 90	<90
függ. frekvencia (Hz)	60	60	50-70	50-70	50-90	50-90
video sávszél. (MHz)	14.3-16.3	14.3-16.3	28	28	< 100	< 100

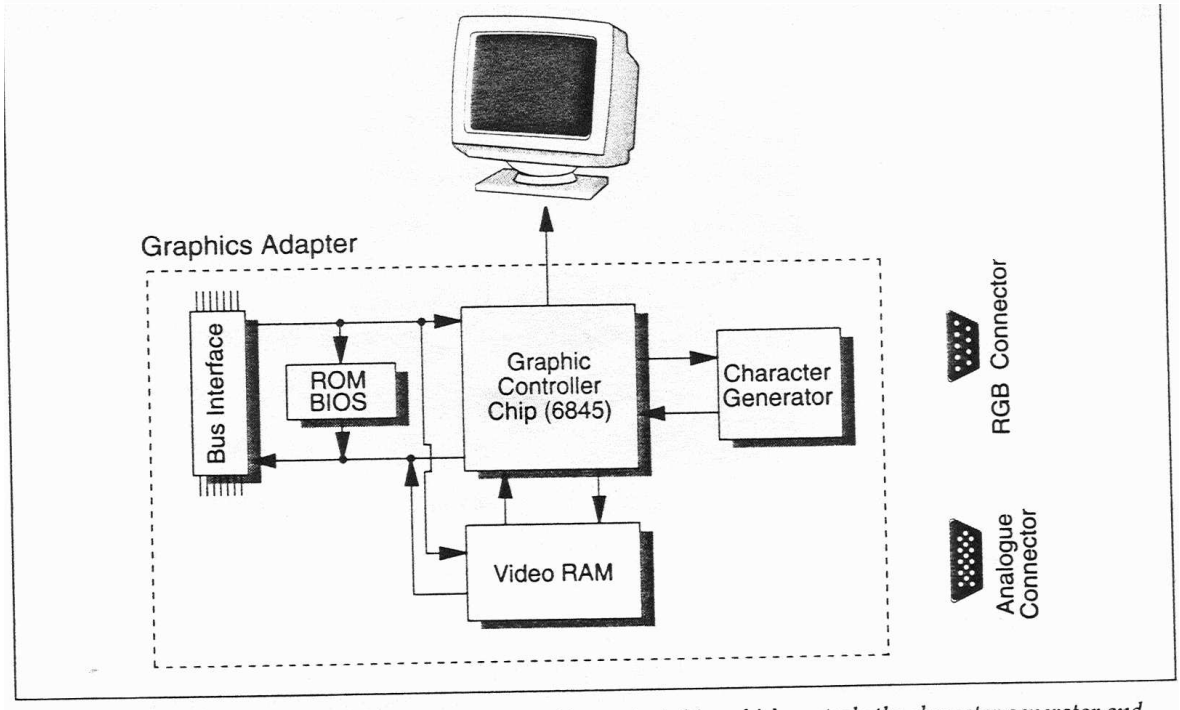


Figure 1.9: Graphics adapter. The central part is a graphics control chip, which controls the character generator and the video RAM. The CPU can access the control chip and the video RAM via the bus interface.

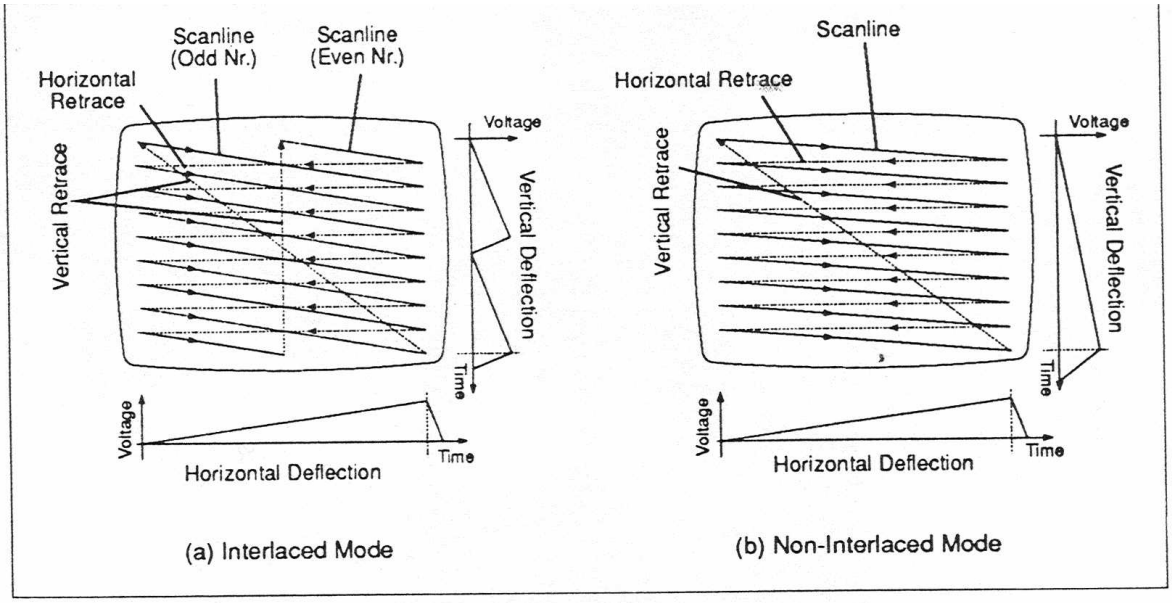
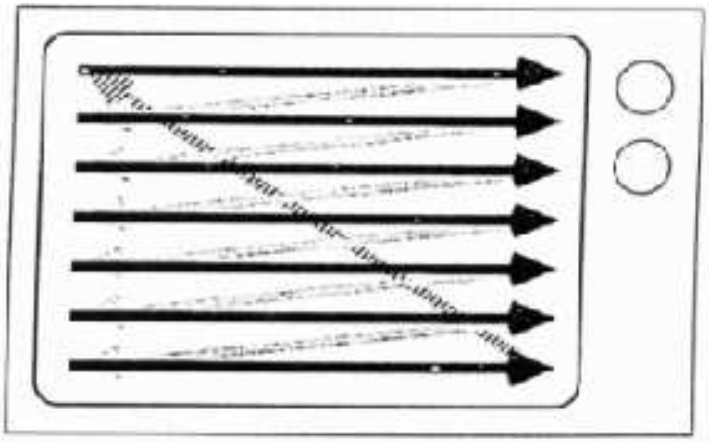
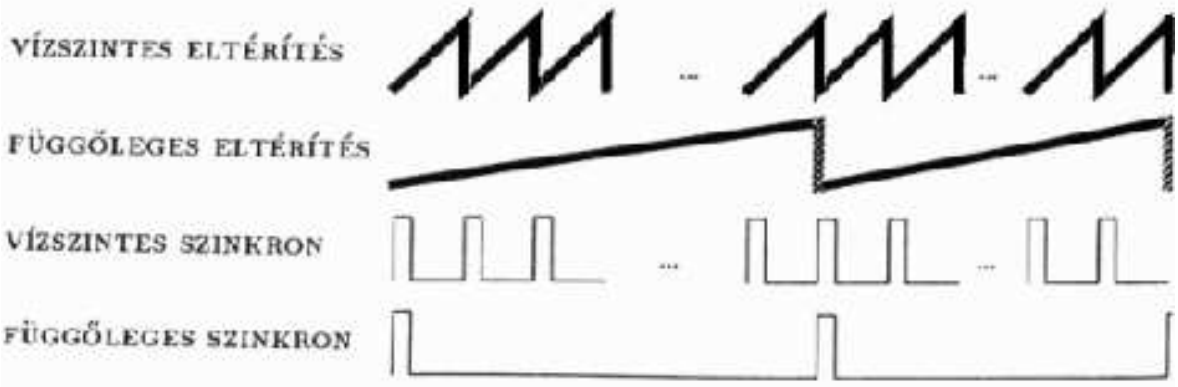
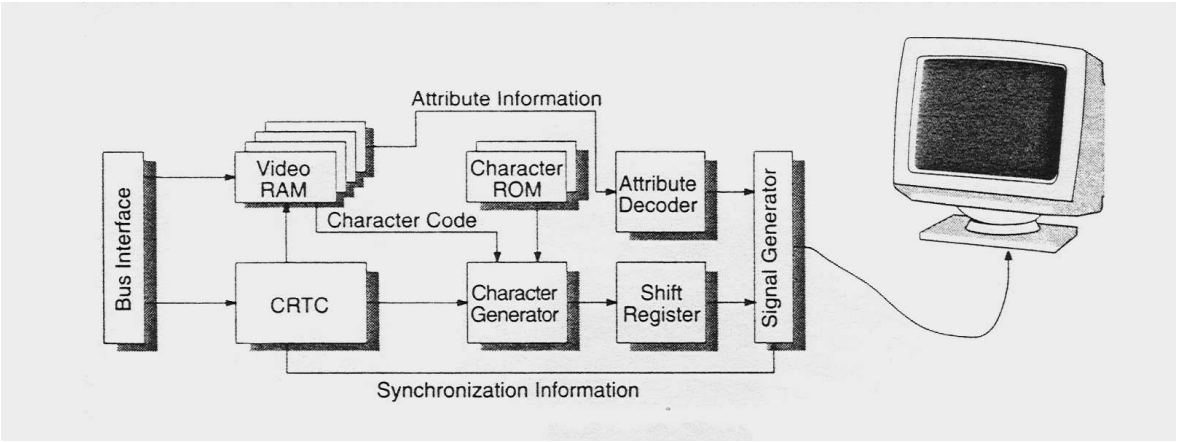


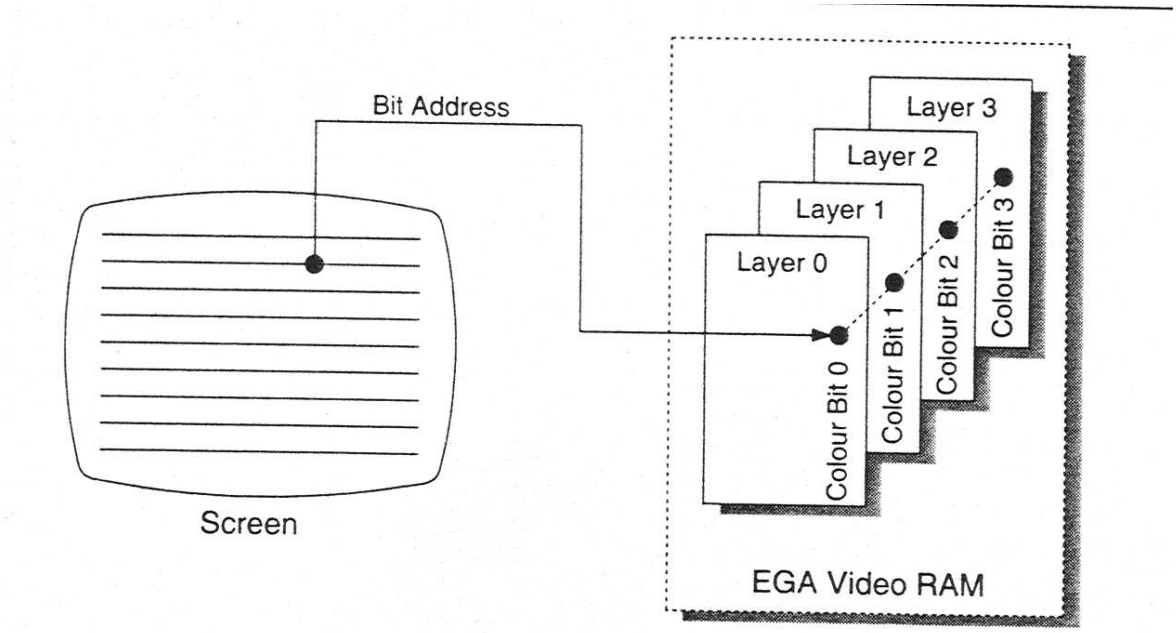
Figure 32.2: Interlaced and non-interlaced mode. (a) In interlaced mode, the scanlines with an odd number are first written, and then all scanlines with an even number. The voltage of the vertical deflection unit carries out two cycles for one complete image; (b) in non-interlaced mode the lines are written in succession.



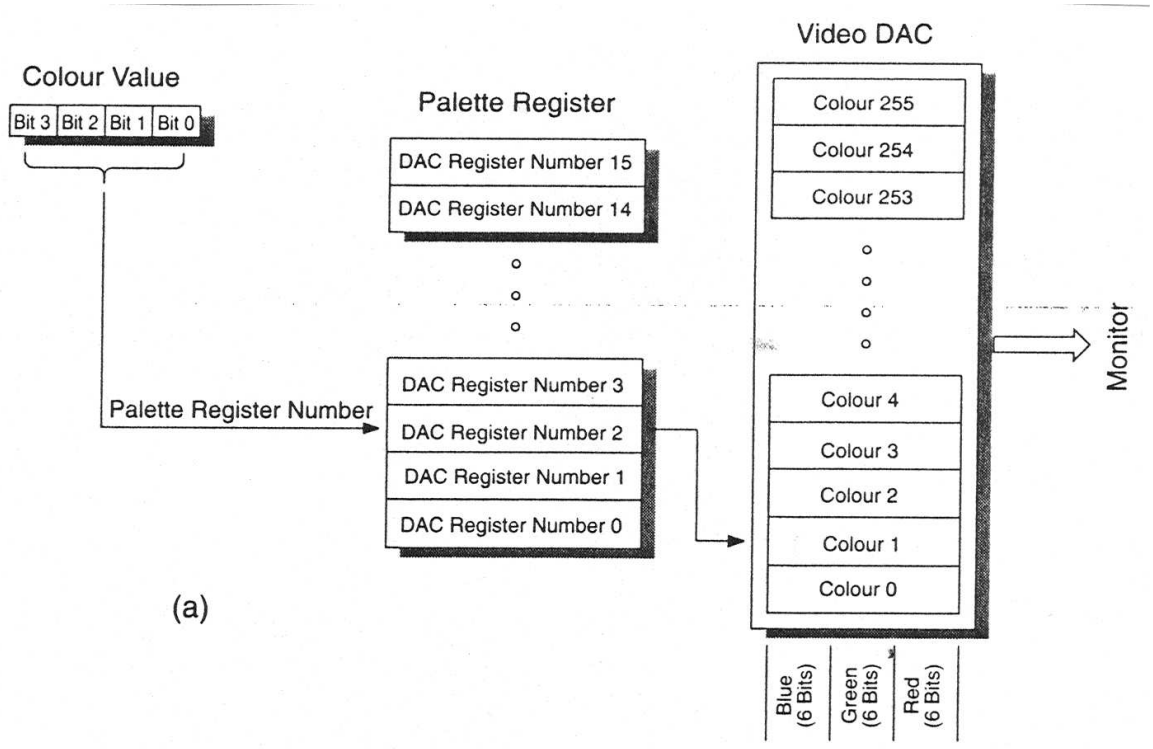

VÍZSZINTES ELTÉRÍTÉS
FÜGGŐLEGES ELTÉRÍTÉS
VÍZSZINTES SZINKRON
FÜGGŐLEGES SZINKRON

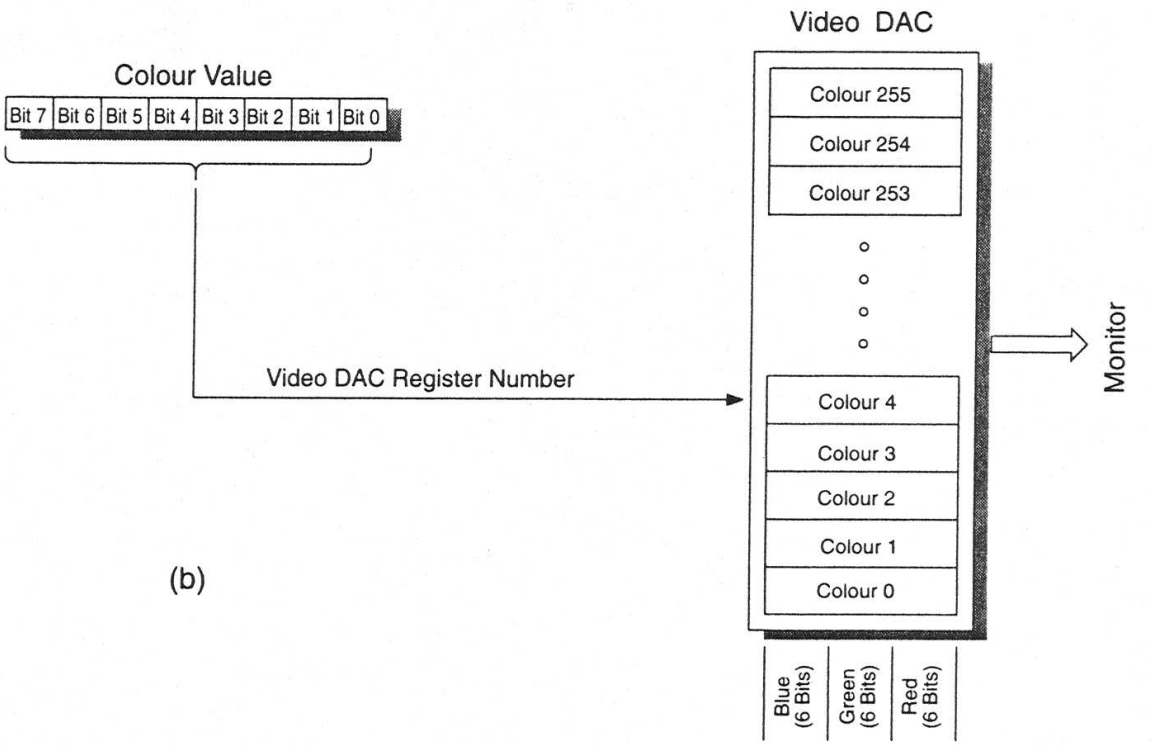
8.5.1. ábra


Attribute Information
Video RAM
Character ROM
Attribute Decoder
Character Code
Bus Interface
CRTC
Character Generator
Shift Register
Signal Generator
Synchronization Information



Distribution of the 4 bit/pixel to the memory layers in EGA modes 13, 14 and 16.

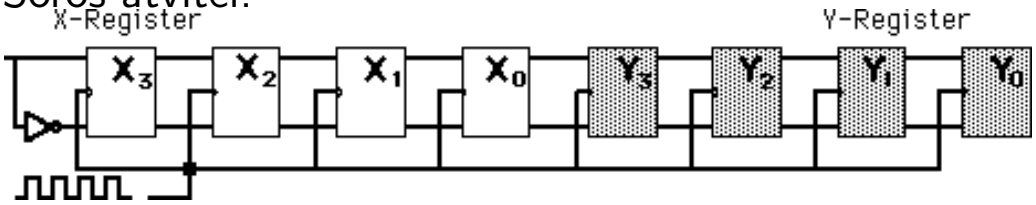

Video DAC
Colour Value
Bit 3
Bit 2
Bit 1
Bit 0
Palette Register
DAC Register Number 15
DAC Register Number 14
DAC Register Number 3
DAC Register Number 2
DAC Register Number 1
DAC Register Number 0
Palette Register Number
Colour 255
Colour 254
Colour 253
Colour 4
Colour 3
Colour 2
Colour 1
Colour 0
Monitor
Blue (6 Bits)
Green (6 Bits)
Red (6 Bits)
(a)



DVI kimenet LCD monitorokhoz

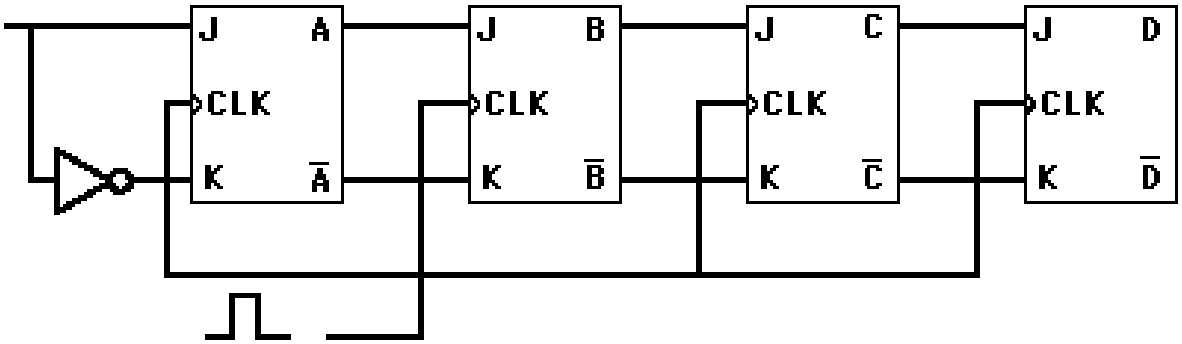
Input és output

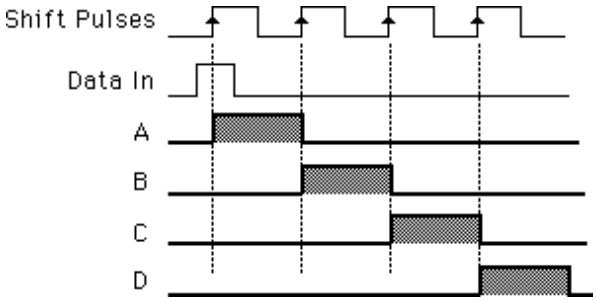
Soros átvitel:



X_3	X_2	X_1	X_0	Y_3	Y_2	Y_1	Y_0
1	1	0	1	0	0	0	0
0	1	1	0	1	0	0	0
0	0	1	1	0	1	0	0
0	0	0	1	1	0	1	0
0	0	0	0	1	1	0	1

Visszaalakítás:





Billentyűzet:

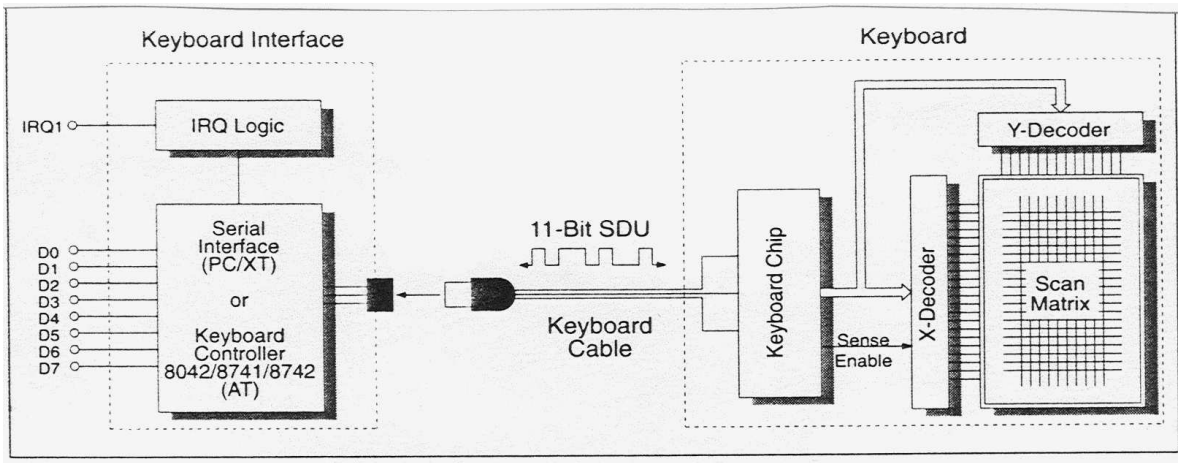
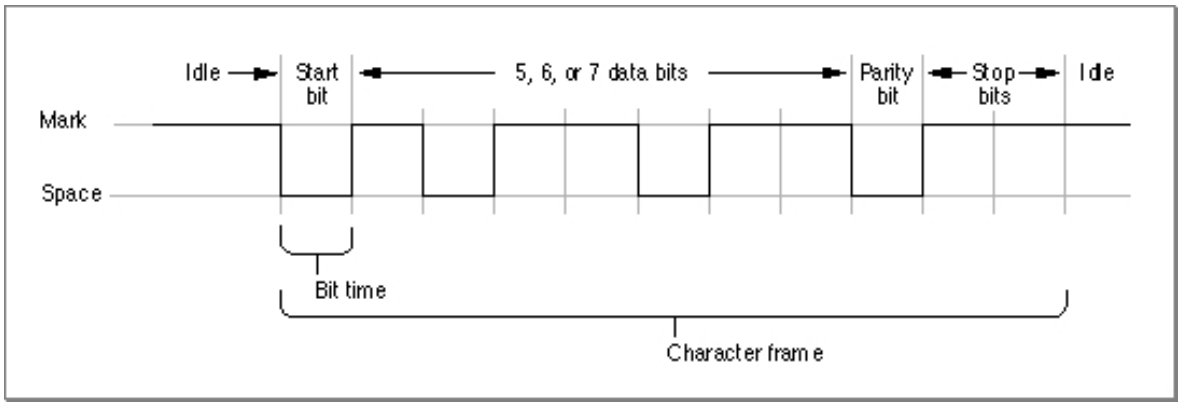
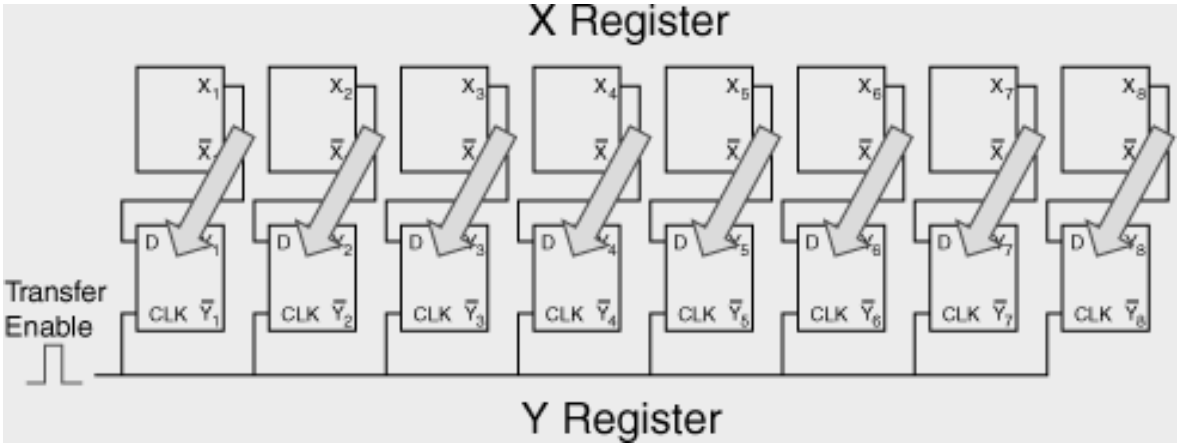


Figure 31.1: Structure of keyboard and keyboard interface.

RS232:


Idle
Start bit
5, 6, or 7 data bits
Parity bit
Stop bits
Idle
Mark
Space
Bit time
Character frame

Parallel átvitel:

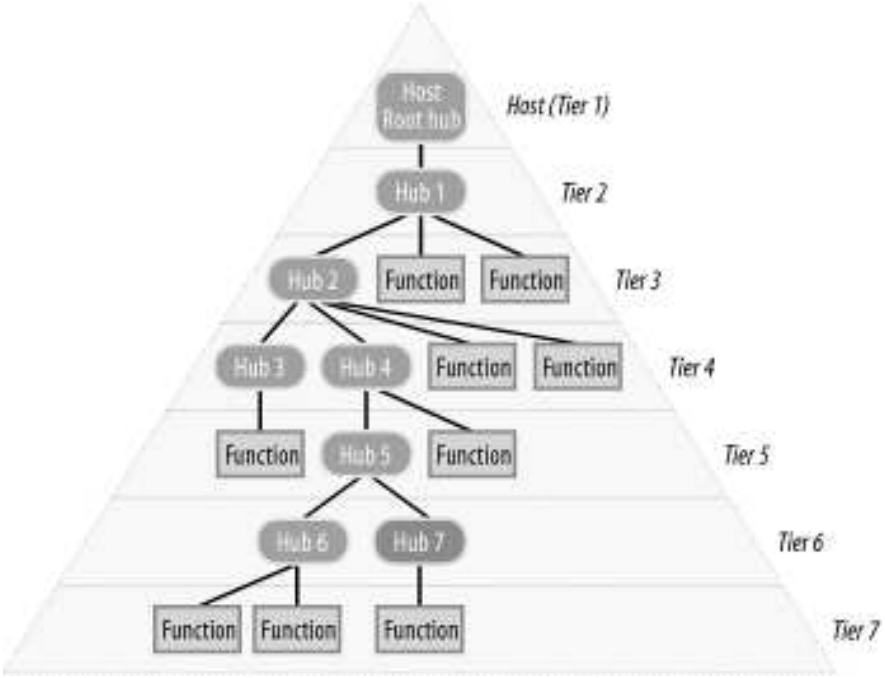


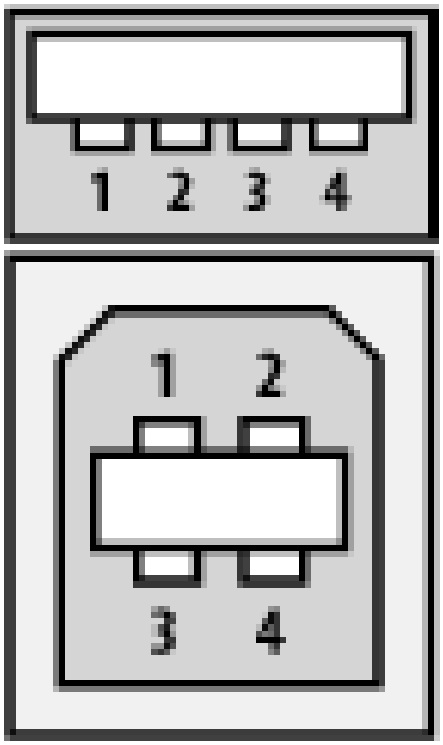
Kapcsolat a buszokkal:
IDE, ATA/PATA, SATA

SCSI

Firewire

USB


Host
Root hub
Host (Tier 1)
Hub 1
Tier 2
Hub 2
Function
Function
Tier 3
Hub 3
Hub 4
Function
Function
Tier 4
Function
Hub 5
Function
Tier 5
Hub 6
Hub 7
Tier 6
Function
Function
Function
Tier 7



Átalakítók:
USB-soros port
USB-parallel port